A Novel ±0.5V Ultra High Current Drive and Output Voltage Headroom Current Output Stage with Very High Output Impedance

Hassan Faraji Baghtash [i *], Ahmad Ayatollahi[ii] and Khalil Monfaredi[iii]

ABSTRACT

A novel ultra-high compliance, low power, very accurate and high output impedance current output stage (COS) with extremely high output current drive capability is proposed in this paper. The principle of operation of this unique structure is discussed, its most important formulas are derived and its outstanding performance is verified by HSPICE simulation in TSMC 0.18μm CMOS, BSIM3, and Level49 technology.

This deliberately composed structure utilizes a well combination (for a mutual auto control action) of negative and positive feedbacks to achieve ever demanded merits such as very low power of 150μW, ultra high ratio of 3000 for output current over the bias current (which is selected to be 0.5μA) at low THD of -20dB and very high output impedance of 5GΩ with power supplies of ±0.5V when operating at class AB mode. Simulation results with ±0.5V power supply shows an absolute output voltage dynamic range of 0.9V which interestingly provides the highest yet reported output voltage compliance for Current mode building blocks implemented by regular CMOS technology. Full process, voltage, and temperature variation (PVT) analysis of the circuit is also investigated in order to approve the well robustness of the structure. The transient stepwise response is also done to verify the proposed COS stability**.**

KEYWORDS

Ultra-low voltage, Ultra-high compliance, Current output stage, Current amplifier, Class AB, High current capability, High output impedance, Low THD

1. INTRODUCTION

Recently low voltage circuit design has been strongly in demand and there has been very much efforts to reduce the power supply of electronic circuits. This is much more enforced by technology down scaling and also encouraged by the fact that the battery-powered and portable equipments are becoming more and more interesting and their versatility is increased expeditiously. The low voltage requirement caused current-mode design approach to have a growing interest and introduce promising results for today's high performance circuits and modern systems. Hence, current-mode techniques have been extensively investigated in recent decades and as a result numerous novel high performance analog, digital and also mixed-mode circuits and systems are presented [1]-[15]. The ever-growing interest in synthesizing the current-mode circuits is mainly due to their more potential advantages such as lower voltage and power consumption, wider dynamic range, inherent wider bandwidth, higher speed, simpler circuitry, smaller nonlinearity and also less complexity which are among the most demanded features of high performance circuits and systems that the designers are always in deal with [1]-[17]. Many active elements capable of operating in current-mode such as output trans-conductance amplifier (OTA), current conveyor, current differencing buffered amplifier (CDBA) and Current-mode operational

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amplifier (COA) have been introduced to response these demands [13]. Current-mode operational amplifier (COA) is one of the useful current-mode integrated building blocks. Current amplifiers are particularly suitable for use with temperature sensors, photo-sensors, and, in general, whenever the input source and or the output are current signals [18].

The main advantage of using COA is its ability to replace with the voltage-mode operational amplifier (VOA) to achieve more qualitative designs while preserving the most aforementioned benefits of the current-mode building blocks [15]. Current output stage (COS) is considered as one of the main blocks of COA and hence its overall performance is directly affect the COA's qualitative performance. The COS block is not only used in COAs but it is also considered as the main part of other analog circuits either in voltage-mode or in current-mode such as operational trans-conductance amplifier (OTA) and voltage to current convertors which are amongst the most versatile analog signal processing systems [3], [11], [12], [18]-[23]. Hence elaborate design and implementation of the COS block is necessary in order to maintain the overall high performance of the system in which it is included. Among the most distinguished features of the COS block are its capability to handle higher output currents with minimum total harmonic distortion (THD) while consuming lower quiescent power, high output impedance and high output voltage headroom.

Conventional types of COS are used in class 'A' mode of operation in order to minimize the THD [18]-[25]. The major drawbacks related to this mode of operation are lower current handling capability which is mainly limited by its bias current and higher power consumption. The alternative approach which can diminish the mentioned disadvantages related to class 'A' scheme is class 'AB' mode of operation [26]-[27]. The proposed circuits in [26]-[27] provide relatively high output impedance but their power supply and power consumption are high which makes them not suitable for today's modern low voltage and also portable applications. On the other hand, they have relatively poor ratio of handled current versus circuit bias current which is degraded much more when the allowable power supply is to be further decreased.

This paper presents a novel ultra-high performance COS that outperforms the previously reported artworks which indebted its high performance to a recently proposed current mirror in which deliberate use of both negative and positive feedback principal enables it to gather some more ever demanded merits of the current mirrors including high output impedance, extremely wide voltage and current dynamic range with very low current transfer error (high linearity), low power supply operation capability and relatively high frequency band width [28]. The proposed circuit is also capable to be used as current amplifier by itself. The proposed circuit's output voltage compliance is the highest yet reported for circuits implemented with regular CMOS technology, while exhibiting low input and extremely high output impedance. The proposed circuit also exhibits a very wide current as well as voltage dynamic range while maintaining a very high accuracy.

Section 2 part A describes the implemented current mirror and the operation of the proposed COS is covered in part B of section 2 and part C is devoted to circuit analysis and formulations. The HSPICE simulation results using TSMC 0.18µm, BSIM3, Level49, CMOS technology are presented in section 3. Finally, section 4 concludes the paper.

2. PROPOSED HIGH PERFORMANCE CURRENT OUTPUT STAGE

A. Current Mirror Principle of Operation

Figure 1 shows a very high performance current mirror proposed recently in [28]. The implemented current mirror consists of a high swing cascode current mirror (M_{n1}-M_{n4}, with M_{n4} transistor connected as diode), M_{n5} as output transistor and an amplifier with gain amplitude of "-An". The high swing cascode is biased with $I_{bn1}=I_{bn2}=I_{bnn}$ currents and its input impedance is reduced using an FVF block at input node and is driven by the input current signal of I_{in}. Both cascode transistors M_{n3} and M_{n4} experience the same bias current, hence V_{dsn1} is set equal to V_{dsn2} prohibiting the channel length modulation effect and thus a very high accurate result is attained. M_{n4}, the diode connected cascode transistor, makes the circuit needless of a separate biasing voltage source. This transistor, on the other hand, provides the input and output nodes with an extra positive feedback loop which increases the performance of the block without using extra circuitry. This structure includes two nested feedback loops in the input side. One of them is a negative shunt feedback implemented with an FVF while another one is a positive series type consists of transistors M_{n1}-M_{n4}. Both loops act simultaneously and are specially devised to reduce the minimum input voltage, $v_{in,min}$, and the input impedance. Similarly, the output side includes two feedback loops, one of them is a negative series one implemented by transistors M_{n4}-M_{n5} and amplifier of '-An' and the next one is a positive shunt feedback consists of transistors M_{n1}-M_{n4}. These two loops act simultaneously and are specially arranged to reduce the minimum output voltage, $v_{out,min}$, and increase the output impedance.

A very simple construction for '-An' gain amplifier suitable for the proposed current mirror can be implemented by only two transistors (configuring a self cascode scheme) and a bias current of I_{bAn} as is shown in Fig. 1.

In conventional method, a negative series feedback is

used to increase the output impedance. This reduces the output compliance by at least $1V_{dsat}$. In other words, the feedback acts while the output voltage is greater than $2V_{dsat}$. By further decreasing the output voltage the feedback gain falls rapidly, causing the output impedance to be decreased rapidly due to the transistors entering the triode region.

Based on conventional definitions, MOS transistor linear region occurs when its output voltage becomes lower than $1V_{DS,sat}=V_{GS}-V_{GS,off}$ (i.e. $V_{DS}< V_{GS}-V_{GS,off}$) which leads to sharp reduction of output current versus voltage reduction. In other words, for a transistor with constant V_{GS} voltage, the channel length modulation causes significant reduction in transistor output resistance. This means that I_{DS} becomes very sensitive to variation of V_{DS} in this region.

According to $I_{DS} = \beta (V_{GS} - V_{TH})^2 (1+\lambda V_{DS})$, the transistor current, I_{DS}, can be varied by both V_{GS} and V_{DS}. When transistor output voltage approaches negative supply, then V_{DS} will decrease causing reduction in transistor current (I_{DS}), of course if V_{GS} remains constant. Now consider the case that V_{GS} can be increased to a value which despite of V_{DS} decrement, maintains the same I_{DS}. Such a case if is arranged then makes the transistor current (I_{DS}) well robust against the output voltage variations. This is exactly what has arranged by the novel structure of the proposed current mirror, Fig. 1, thanks to deliberately composed elements and well combined auto controlled negative and positive feedback in the proposed circuit which made it unique in realizing ultra-high compliances, high output impedance and high accuracy. This is, in fact, a great achievement granted by special feedback arrangement and results a very wide dynamic range which makes the circuit very well suited to be implemented as COS. More detailed information about the current mirror's operation can be found in [28].

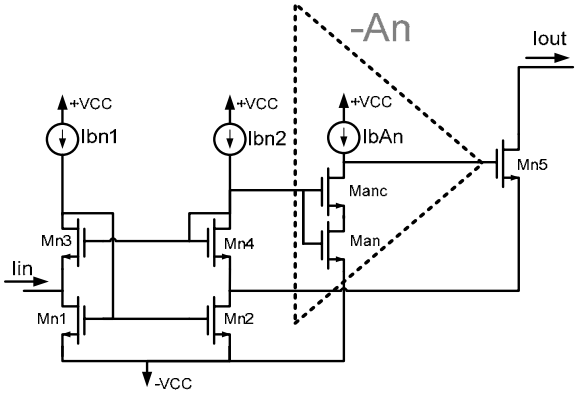

Figure 1: Transistor level schematic of the ultra-high performance current mirror.

B. Proposed COS Principle of Operation

Typical architecture for a COS is shown in Fig.2 which consists of a push-pull follower followed by a complementary current mirror. The COS is made up of a complementary current mirror thus the performance of COS is directly affected by the performance of the implemented current mirror. Current amplifiers always consist of a feedback loop to linearize the transfer function [18].

The complementary current mirror of COS is the main source of nonlinearity when implemented in current amplifier, since it is outside the loop, while the push-pull follower is greatly linearized since it operates inside the loop. The COS's nonlinearity is due mainly to channel modulation effects rather than threshold and geometrical mismatches [18]. High COS performance cannot be achieved using simple current mirrors since they are heavily affected by channel length modulation, which means high nonlinearity and low output resistance. Although some high performance current mirrors such as cascode, regulated cascade, and low voltage regulated cascode current mirrors can be used instead of simple one to improve the qualitative performance of the current amplifier's output stage, they still could not provide the most optimized trade-offs required due to their drawbacks in terms of input and output swing, low output impedance and input/output voltage head rooms, low output current dynamic range that makes them impractical for high current applications, and high power supply which makes them not suitable for low voltage applications. On the other hand, the maximum output current is limited by the quiescent bias current which is a major issue when the low voltage applications are demanded.

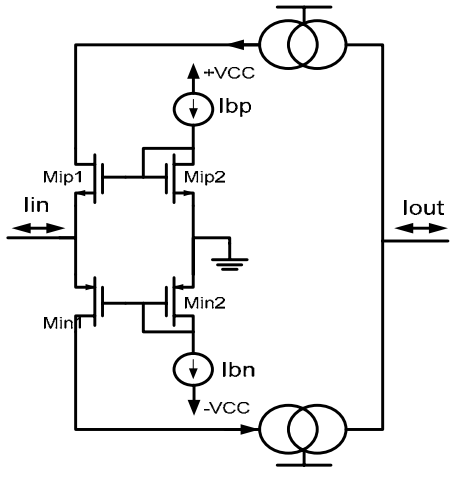

Figure 2: Typical architecture for a current amplifier.

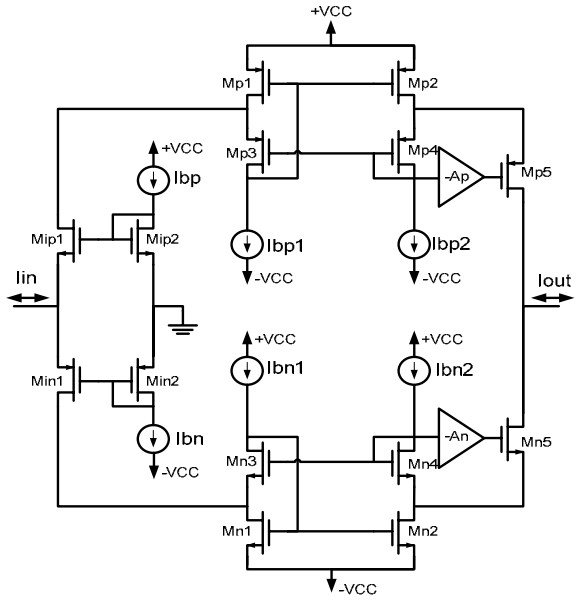

Figure 3: The conceptual schematic of a class 'AB' COS.

Figure 3 shows the conceptual schematic of a class 'AB' COS implemented with the very high performance current mirror described in previous part. The proposed current output stage outperforms the previously reported ones and is a promising solution for very high performance applications as well as very low voltage high dynamic range circuits and systems.

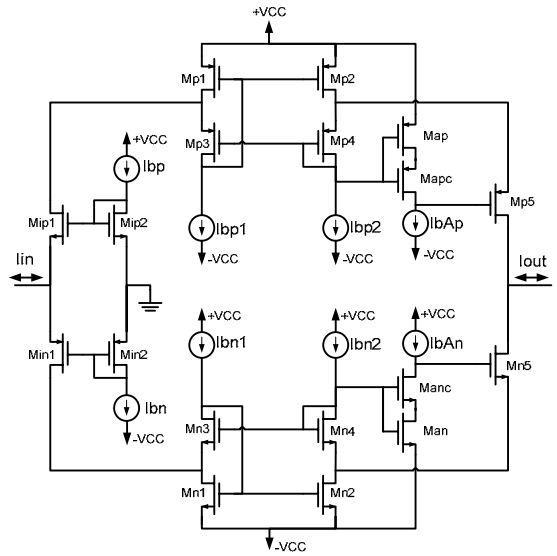

Figure 4: The transistor level schematic of a class 'AB' COS.

The proposed COS, which its transistor level schematic is shown in Fig. 4, consists of push-pull follower (M_{in1}-M_{in2}, M_{ip1}-M_{ip2}, Ibn and Ibp), followed by the extremely high performance complementary current mirror.

The implemented current mirror which is described in previous part for N-type along with the same half for P-type one, makes the class AB operation of the current amplifier possible.

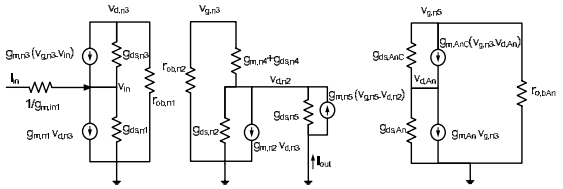

Figure 5: Half small signal equivalent circuit.

C. Circuit Analysis

The Half small signal equivalent circuit of the Fig. 4 is shown in Fig. 5. Analytical formulations to extract parameters of the proposed circuit are performed in the following subsections based on half small signal equivalent circuit of Fig. 5 assuming that the source of each transistor is connected to its body. The simulations are also performed based on this assumption.

Output impedance analysis

In the following analysis, g_m, r_o and g_{ds} stand for the trans-conductance, the output resistance and the output conductance of the transistors, respectively. The transistors' numbers are indicated as subscripts of these parameters.

Performing some analysis and doing necessary simplifications [28], output impedance is then approximated as (1):

$$R_{out,n} \cong \frac{g_{m,n5} \times r_{o,n5} \times (An+1) \times \left(r_{ob,n2} \| r_{o,n2}\right)}{1 - \frac{g_{m,n2} \times g_{m,n3} \times \left(r_{ob,n2} \| r_{o,n2}\right)}{g_{m,n1}}} \quad (1)$$

where 'An' is given by (2):

$$An \cong g_{m,An} \times \left(\frac{g_{m,AnC}}{g_{ds,An} \times g_{ds,AnC} + g_{ds,bAn} \times g_{m,AnC}} \| r_{o,bAn} \right) \quad (2)$$

Performing the same analysis for P-type half of the proposed structure gives $R_{out,p}$ as:

$$R_{out,p} \cong \frac{g_{m,p5} \times r_{o,p5} \times (Ap+1) \times \left(r_{ob,p2} \| r_{o,p2}\right)}{1 - \frac{g_{m,p2} \times g_{m,p3} \times \left(r_{ob,p2} \| r_{o,p2}\right)}{g_{m,p1}}} \quad (3)$$

where 'Ap' is given by (4):

$$Ap \cong g_{m,Ap} \times \left(\frac{g_{m,ApC}}{g_{ds,Ap} \times g_{ds,ApC} + g_{ds,bAp} \times g_{m,ApC}} \| r_{o,bAp} \right) \quad (4)$$

The total output impedance of the proposed circuit is given by (5):

$$R_{out} \cong R_{out,n} \| R_{out,p} \quad (5)$$

From (1) and (3) it is derived that the output resistance is capable to have negative or positive values. Also, assuming ideal circumstances for the fabrication process an infinite resistance seems to be achievable by adjusting the transistors' aspect ratios. In most applications, negative resistance is undesired thus to avoid this condition the relation (6) should be satisfied.

$$1 \geq g_{m,n3}\left(r_{ob,n2} \| r_{o,n2}\right) \quad and \quad 1 \geq g_{m,p3}\left(r_{ob,p2} \| r_{o,p2}\right) \qquad (6)$$

In this work, (6) is satisfied by: 1) Making $g_{m,n3}$ ($g_{m,p3}$) sufficiently small via choosing small W_{3n}/L_{3n} (W_{3p}/L_{3p}) and W_{4n}/L_{4n} (W_{4p}/L_{4p}). 2) Biasing M_{n1} (M_{p1}) and M_{n2} (M_{p2}) in their triode region which cause $r_{o,n1}$ ($r_{o,p1}$) and $r_{o,n2}$ ($r_{o,p2}$) to be sufficiently small. These arrangements also help the current mirror to present high input and output compliances.

Input impedance analysis

Performing some analysis and doing necessary simplifications [28], input impedance is then approximated as (7):

$$R_{in,n}=\frac{1}{g_{m,in1}}+\frac{g_{m,n5}\times g_{ds,n3}\times g_{ds,n1}\times(An+1)-g_{m,n1}\times g_{m,n3}^2}{g_{m,n1}\times g_{m,n3}^2\times g_{m,n5}\times(An+1)}=\frac{1}{g_{m,in1}} \qquad (7)$$

Performing the same analysis for P-type half of the proposed structure gives $R_{in,p}$ as:

$$R_{in,p}=\frac{1}{g_{m,ip1}}+\frac{g_{m,p5}\times g_{ds,p3}\times g_{ds,p1}\times(Ap+1)-g_{m,p1}\times g_{m,p3}^2}{g_{m,p1}\times g_{m,p3}^2\times g_{m,p5}\times(Ap+1)}=\frac{1}{g_{m,ip1}} \qquad (8)$$

The total input impedance of the proposed circuit is given by (9):

$$R_{in}\cong R_{in,n}\|R_{in,p} \qquad (9)$$

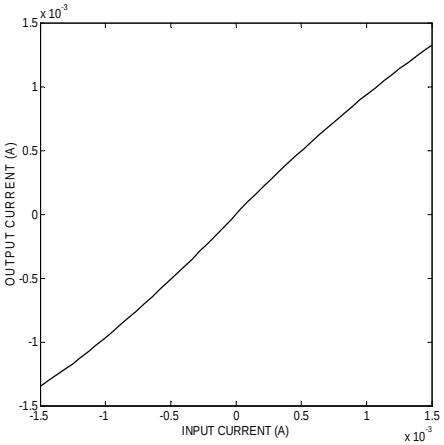

Figure 6: Current transfer function dynamic range of the proposed COS structure.

3. SIMULATION RESULTS

HSPICE simulations are carried out using TSMC 0.18µm, BSIM3, Level49, and CMOS technology utilizing ±0.5V power supply. Bias currents of I_{bn} (I_{bp}), I_{bnn} ($I_{bp1}=I_{bp2}=I_{bpp}$) and I_{bAn} (I_{bAp}) are taken to have values of 0.5µA, 5µA and 2.5µA respectively. I_{in} is taken to have DC value of 10µA for PVT analysis. Fig.6 shows the output current versus input current sweep. It is shown that the current dynamic range of the proposed circuit is extremely wide and is about in the range of ±1.5mA which is favorably 3000 times larger than bias current of I_{bn} (I_{bp}). Favorably the current transfer error remains below -20dB for currents up to ±1.5mA. Figure 7 shows the DC output characteristics with V_{out} swept from -0.5V to 0.5V and I_{in} stepped from -25 µA to 25µA in steps of 1µA. As is shown in this figure, the proposed circuit exhibits extremely high output resistance of 5GΩ along with much higher compliance voltage which proves the well functionality of embedded positive feedback that makes the structure suitable for ultra-low voltage applications. This figure also proves very high accuracy of output current together with negligible current offset which makes the structure very preferable for modern ultra-high precision applications. Another more interesting characteristic of circuits is dynamic range which is depicted in Fig. 7 and validates the superior performance of proposed circuit. Favorably the output voltage of the proposed circuit uses only 0.05V from supply voltages to operate in high impedance region leaving very outstanding value of 0.9V output voltage headroom, which promises ultra-high compliances at the output node.

The output current transient step response of the proposed COS structure is shown in Fig. 8 to validate the structures stability. Figure 9 shows THD (%) of the proposed COS circuit in terms of sinusoidal input current with frequencies swept from 100K up to 100M and signal amplitude swept from 10 µA up to 500µA. The proposed COS is capable of operating as COA by itself just by adjusting its mirror transistors aspect ratios. This capability is verified by Fig. 10 and Fig. 11 in DC current transfer curve and frequency domain response, respectively. The total power consumption of the proposed current mirror is about 150µW. Compared results are summarized in Table.1. For simulating the practical fabrication condition, the Monte Carlo analysis is performed applying 5% mismatch in transistors aspect ratios and threshold voltage with Gaussian distribution. The Monte Carlo simulation results are shown in Fig. 12. In order to further investigate the performance of the proposed circuit against PVT variations, it is also simulated for various temperatures (-25, 0, 25, 50 and 75 centigrade degree) and ±10% variations of supply voltages. The results are depicted in Figures 13 and 14. These figures show that the fabrication process does not have significant effect on proposed circuit's performance which is another excellent achievement of the circuit.

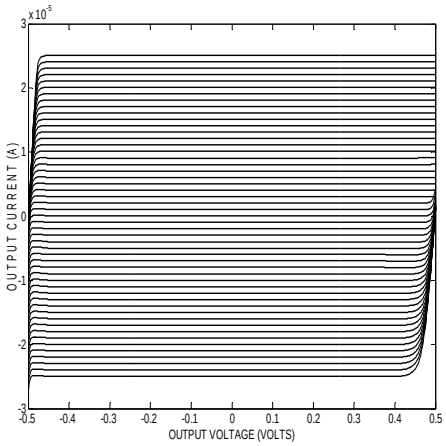

Figure 7: Output voltage of the proposed COS structure in terms of output current with input current swept from -25µA up to 25µA in 1µA steps.

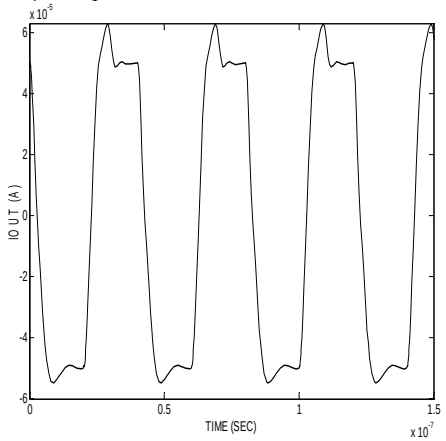

Figure 8: The transient step response of the proposed COS structure.

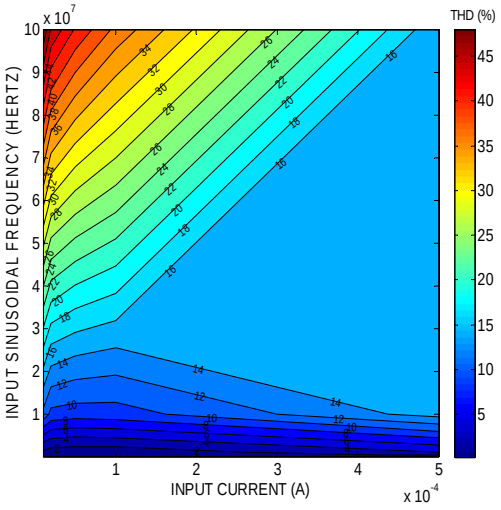

Figure 9: Total harmonic distortion of the proposed COS structure in terms of sinusoidal input current.

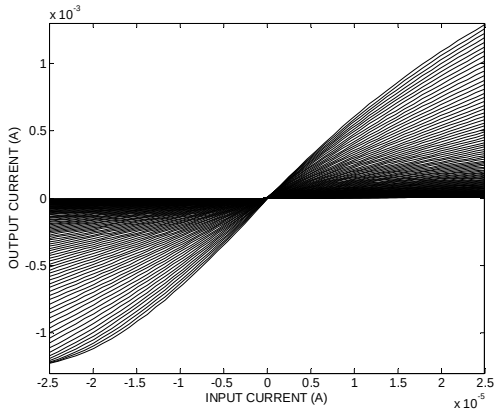

Figure 10: Current transfer function of the proposed COS structure for various gains.

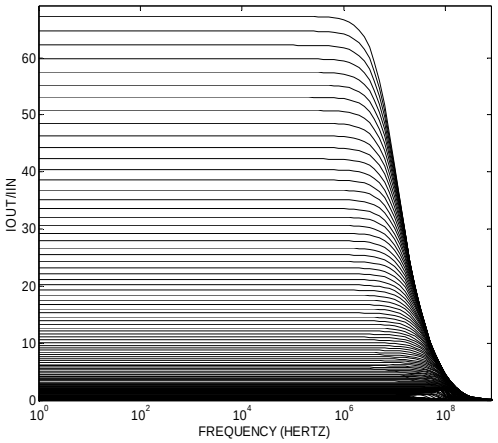

Figure 11: Frequency response of the proposed COS structure for various gains.

4. CONCLUSION

A novel ultra-high compliance, low power, very accurate and high output impedance COS with extremely high output current drive capability is proposed. The principle of operation of this unique structure is discussed, its most important formulas are derived and its outstanding performance is verified by HSPICE simulation in TSMC 0.18µm CMOS, BSIM3, and Level49 technology.

The circuit interestingly achieves ever demanded merits such as very low power of 150µW, ultra high ratio of 3000 for output current over the bias current (which is selected to be 0.5µA) at low THD of -20dB and very high output impedance of 5GΩ with power supplies of ±0.5V when operating at class AB mode. Simulation results with ±0.5V power supply shows an output voltage dynamic range of 0.9V which interestingly provide the highest yet reported voltage compliance for Current mode building blocks implemented by regular CMOS technology. Full PVT variation analysis of the structure is also investigated in order to approve the well robustness of this stage. The transient stepwise response is also done to verify the proposed COS stability.

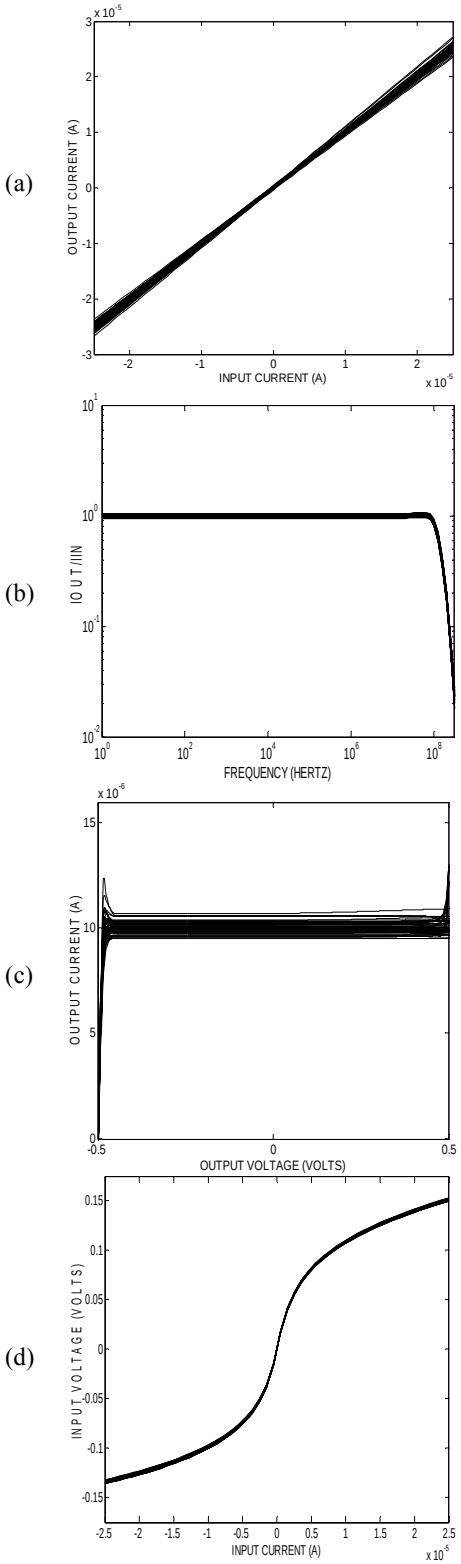

Figure 12: Monte Carlo analysis of the proposed COS structure (a) current transfer function, (b) frequency response, (c) output current in terms of output voltage variation, and (d) input voltage in terms of input current variation.

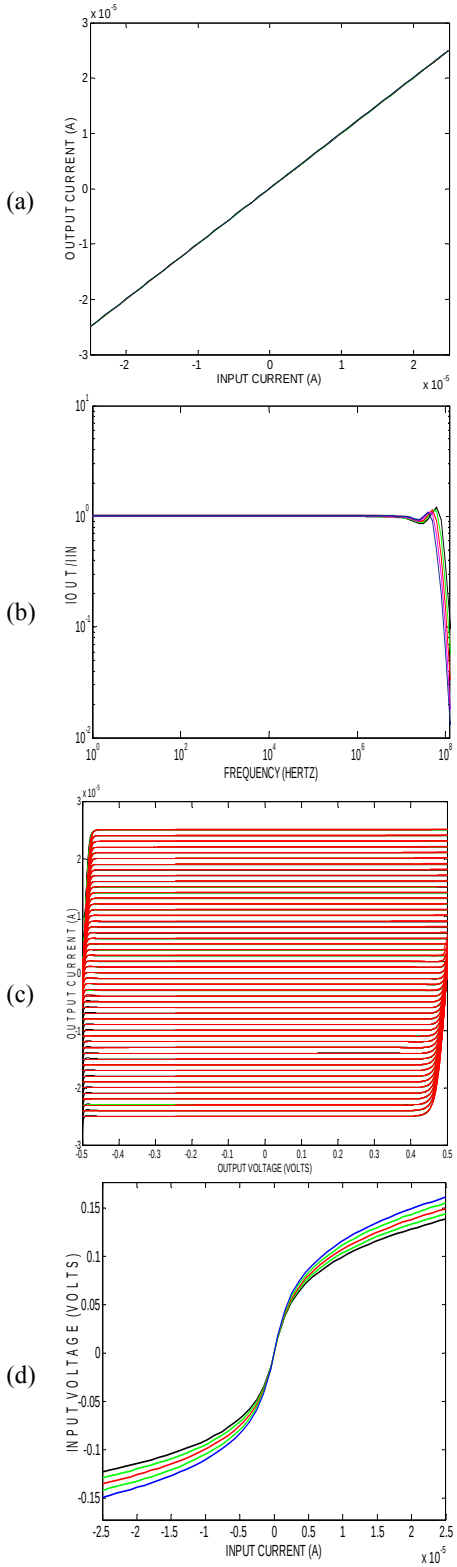

Figure 13: Temperature analysis of the proposed COS structure (a) current transfer function, (b) frequency response, (c) output current in terms of output voltage variation, and (d) input voltage in terms of input current variation.

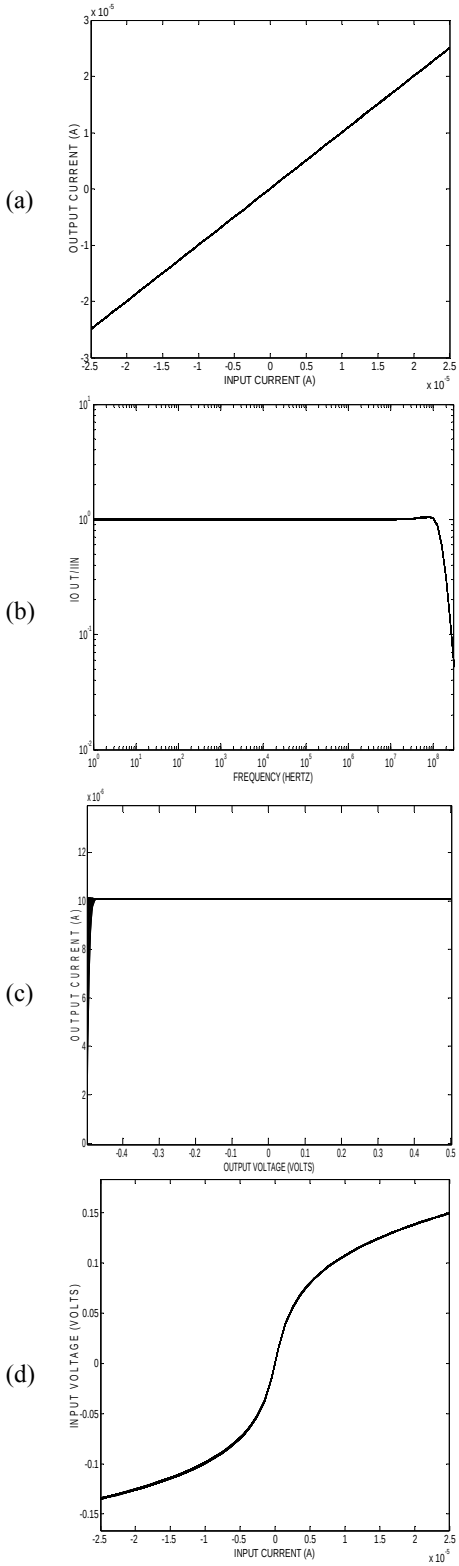

Figure 14: VDD variations analysis of the proposed COS structure (a) current transfer function, (b) frequency response, (c) output current in terms of output voltage variation, and (d) input voltage in terms of input current variation.

TABLE 1
COMPARATIVE PARAMETERS OF THE PROPOSED COS WITH OTHER RECENT WORKS.

REFERENCE	[23] Fig2-c	[24]	[25]	[26]	[27]	THIS WORK
Power supply	4v	5v	±2v	±2v	2.5v	±0.5v
Power	900 µw	NA	560 µw	57 µw	51.2 µw	150µw
Current capability	50µA	100 µA	35 µA	100 µA	NA	±1.5 mA
-3dB frequency	NA	20Mhz	NA	17Mhz	28 Mhz	~100Mhz
Output impedance	50KΩ	NA	NA	25GΩ	5 GΩ	5GΩ
THD	NA	NA	-36dB	-50dB	NA	-20dB @ 1.5mA
Technology (CMOS)	0.35um	0.8um	0.13um	0.8um	0.8um	0.18um

5. REFERENCES

[1] C. Toumazou, F. J. Lidgey and D. G. High, Analog IC Design: The Current Mode Approach. London: Peter Peregrinus Ltd., 1993.

[2] Chang-Hyeon Lee, Jack Cornish, Kelly McClellan, and John Choma, "Current-mode approach for wide gain-bandwidth product architecture," IEEE trans. on CAS-II, vol. 45, pp. 229 – 232, May 1998.

[3] G. Palmisano, C. Palumbo, and S. Pennisi, CMOS Current Amplifiers. Boston: Kluwer Academic Publishers, 1999.

[4] Luis N. Alves, Rui L. Aguiar, "A differential current-conveyor based buffer for high-bandwidth, low-signal applications," in Proc. 1999 IEEE Conference on Electronics, Circuits and System (ICECS'99), pp. 903 – 906.

[5] Hesham F. Hamed, Ahmed El-Gaafary and Mostafa S. A. El-hakeem, "A new differential current conveyor and its application as a four quadrant multiplier," in Proc. 2001 IEEE Int. Conference on Electronics, Circuits and Systems, pp. 569-572.

[6] Salvatore Pennisi, "A low-voltage design approach for class AB current-mode circuits," IEEE Transactions on circuits and systems—II: Analog and digital signal processing, vol. 49, pp. 273–279, April 2002.

[7] R. Sennani, and S. S. Gupta, "Novel sinusoidal oscillators using only unity voltage followers and current followers," IEICE Electron. Express, vol. 1, pp. 404-409, October 2004.

[8] Y. S. Hwang, L. P. Liao, C. C. Tsai, W. T. Lee, and T. Y. Lee, "A new CCII-based pipelined analog to digital converter," in Proc. 2005 IEEE International Symposium on Circuits and Systems (ISCAS), Japan, pp. 6170-6173.

[9] M. Alioto, G. Palumbo, Model and design of Bipolar and MOS Current-Mode logic: CML, ECL and SCL Digital Circuits. Dordrecht: Springer, 2005.

[10] Jaroslav Koton, Kamil Vrba, and Pavel Hanak, "Frequency filter with current conveyors for signal processing of data-buses working in the current-mode," in Proc. 2006 International Conference on Networking, International Conference on Systems and International Conference on Mobile Communications and Learning Technologies (ICNICONSMCL'06), pp. 156-159.

[11] Mahmut Tokmakci, "The comparative analysis of current mirror based cmos current amplifiers," IEICE Electronics Express, vol. 4, pp. 411-416, July 2007.

[12] M. Altun, and H. Kuntman, "Design of a fully differential current mode operational amplifier with improved input- output impedances and its filter applications," International Journal of Electronics and Communication, vol. 62, pp. 239-244, March 2008.

[13] Montree Siripruchyanun, and Winai Jaikla, "CMOS current-controlled current differencing transconductance amplifier and applications to analog signal processing," Int. J. Electron. Commun (AEÜ), vol. 62, pp. 277 – 287, Dec 2008.
[14] H. P. Chen, and P. L. Chu, "Versatile universal electronically tunable current mode filter using CCIIs," IEICE Electronics Express, vol. 6, pp. 122-128, 2009.
[15] Mustafa Altun, and Hakan Kuntman, "Design of a fully differential current mode operational amplifier with improved input–output impedances and its filter applications," Int. J. Electron. Commun. (AEÜ), vol. 62, pp. 239 – 244, March 2008.
[16] G. Palmisano, G. Palumbo, and S. Pennisi, "Harmonic distortion on class AB CMOS current output stages," IEEE Transactions on circuits and systems—II: analog and digital signal processing, vol. 45, pp. 243-250, February 1998.
[17] D. R. Bhaskar, V. K. Sharma, M. Monis, S. M. I. Rizvi. "New currentmode universal biquad filter," Microelectron. J., vol. 30, pp. 837–839, January 1999.
[18] G. Palmisano, G. Palumbo, and S. Pennisi "High linearity CMOS current output stage," Electronics letters, vol. 31, pp. 789-790, 1995.
[19] Giuseppe Di Cataldo, Rosario Mita, Salvatore Pennisi, "High-speed CMOS unity-gain current amplifier," Microelectronics Journal, vol. 37, pp. 1086–1091, June 2006.
[20] Arie F. Arbel, "Output stage for current-mode feedback amplifiers, theory and applications," Analog Integrated Circuits and Signal Processing, vol. 2, pp. 243-255, Sep. 1992.
[21] I. Mucha, "Current operational amplifiers: Basic architecture, properties, exploitation and future," Analog Integrated Circuits and Signal Processing, vol. 7, pp. 243-255, 1995.
[22] S. Pennisi, M. Piccioni, G. Scotti, A. Trifiletti, "High-CMRR current amplifier architecture and its cmos implementation," IEEE Transactions on Circuits and Systems II: Express Brief, vol. 53, pp. 1118-1122, Oct. 2006.
[23] F. Centurelli, A. D. Grasso, S. Pennisi, G. Scotti, and A. Trifiletti, "CMOS high-CMRR current output stages," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 54, pp. 745-749, Sep. 2007.
[24] F. Centurelli, S. Pennisi, and A. Trifiletti, "Current output stage with improved CMRR," in Proc. 2003 IEEE International Conference on Circuits and Systems, pp. 543 - 546.
[25] M. H. Kashtiban, and S. J. Azhari, "A novel high CMRR low voltage current output stage," in Proc. 2009 International Symposium on Signals, Circuits and Systems (ISSCS), pp. 1-4.
[26] G. Palumbo, and S. Pennisi, "Low-voltage class AB CMOS current output stage," Electronics Letters, vol. 35, pp. 1329-1330, 1999.
[27] A. Zeki, and H. Kuntman, "High-linearity low-voltage self-cascode class AB CMOS current output stage," in Proc. 2000 IEEE International Symposium on Circuits and Systems (ISCAS), Geneva, pp. 257-260.
[28] S. J. Azhari, H. F. Baghtash, and K. Monfaredi, "A novel ultra-high compliance, high output impedance low power very accurate high performance current mirror," Microelectronics Journal, Vol.42, No. 2, Pages 432-439, February 2011.