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Low-Power MOSFET-Only Subthreshold Voltage Reference with High PSRR

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ABSTRACT: This work presents a sub-nanowatt voltage reference (VR) achieving a high-power supply ripple rejection (PSRR). It utilizes a self-current biasing circuit to reduce the voltage dependency of the output voltage (V_{REF}) to the power supply variations. For low-power operation, all transistors operate in the subthreshold region. The design's performance is verified through post-layout and Monte Carlo simulations in a standard 180 nm CMOS process. Results show that the proposed bandgap achieves an output voltage of 0.150 V with a PSRR of -81.5 dB at V_{dd} = 1V. Notably, it eliminates the need for an additional startup circuit and consumes only 0.72 nW at T = 27°C with Vdd = 0.5V. The proposed voltage reference exhibits a temperature coefficient (TC) of approximately 18 ppm/°C over a temperature range of -20°C to 130°C while without using a trimming circuit a reasonable (σ_{VREF}/μ_{VREF}) = 2.3% is obtained. This design's average line sensitivity (LS) is 0.072%/V (V_{dd} = 0.5V to 1.8V). However, the PSRR and LS values are temperature-dependent. At the high temperature of 130°C (worst-case), the PSRR and LS degrade to approximately -80.45 dB and 0.084 %/V, respectively. The output noise at the frequency of 1 KHz is obtained as 167.34 nV/ √ Hz. The proposed VR occupies a small active area of 513.5 µm².

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1- Introduction

In today's world, with enormous developments in areas such as the Internet of Things and wireless technology, the demand for low-power and low-voltage circuits is rapidly increasing [1, 2]. Voltage references are critical components in various electronic devices, including analog-to-digital converters, biomedical devices, and remote environmental monitoring systems. These devices often rely on batteries or solar power, which can be affected by environmental conditions and battery degradation, leading to unstable supply voltages. Therefore, a voltage reference with excellent LS is crucial for maintaining accurate and reliable operation in these applications. This paper presents a low-power VR with a high LS to address these challenges. The bandgap reference (BGR) is a traditional type of VR. It can generate a reference voltage (V_{REF}) which has a small TC, but it is difficult to operate at low supply voltage and low power consumption [3-5]. Conventional CMOS Bandgap Reference (BGR) circuits typically generate their output voltage using resistors and lateral PNP bipolar junction transistors (BJTs) [6, 7]. Due to the demand for low-power circuits, new low-power approaches have been presented in these years [8-11]. The VR presented in [2, 9, 12] utilizes a CMOS self-cascode configuration to generate a voltage proportional to absolute temperature (PTAT), while the base-emitter voltage (V_{BE}) is used as a complementary to absolute temperature (CTAT) voltage source. Another VR design uses the subtraction of two PTAT voltages with different slopes to obtain the desired reference voltage [13].

Subthreshold VRs are a preferred choice for low-power applications. In the subthreshold region, the drain current (I_D) of MOSFETs exhibits an exponential dependence on the gate-source voltage (V_{GS}), similar to bipolar junction transistors (BJTs). This characteristic allows the generation of the PTAT voltage by exploiting the V_{GS} difference between two MOSFETs, as used in [12, 14, 15]. Building on this concept, reference [16] introduces a two-transistor CMOS voltage reference where one of the transistors (M_2) is a native nMOS device with a near-zero threshold voltage, as shown in Fig. 1. The design utilizes various MOS devices operating in the subthreshold region. The design in [16] is made up of two different transistors. M_2 is a native transistor and M_1 is a thick oxide input/output (I/O) device. Hence, the subthreshold drain current can be expressed by (1) when V_{ds} is greater than 0.1V [8, 17]:

$$K\mu_n C_{ox}(m-1)V_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) \quad (1)$$

K the device aspect ratio, is defined by the ratio of the

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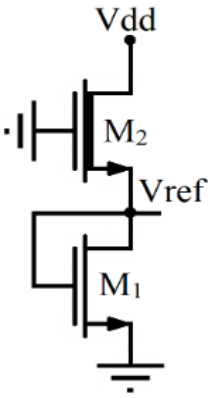


Fig. 1. Two transistor CMOS VR in [16].

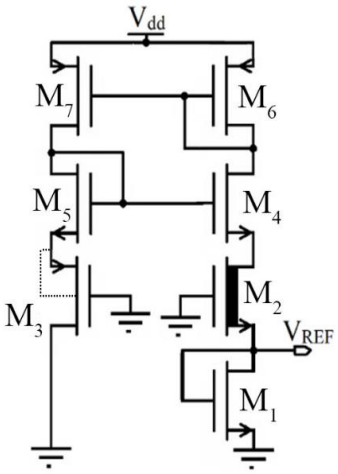


Fig. 2. Proposed voltage reference circuit.

transistor's width (W) to its length (L). μ_n is the electron mobility and C_{ox} is the oxide capacitance per unit area. m is the subthreshold slope factor, V_T is the thermal voltage, V_{GS} and V_{TH} are the gate-source and threshold voltages of the transistor, respectively. Since transistor, M_2 connects directly to V_{dd}, its limited output resistance affects the current flowing through both M_1 and M_2. This, in turn, leads to some degree of power supply dependence on the output voltage. As a result, this design has limitations in achieving good LS and PSRR.

Based on the work presented in [16], this paper proposes a subthreshold VR that utilizes self-current biasing to significantly reduce its dependence on supply voltage variations. The proposed VR offers significant improvements in LS and PSRR compared to the design in [16]. The structure of this paper is as follows. Chapter II introduces the proposed circuit and its design considerations. Chapter III presents the simulation results which demonstrate the improved performance of the proposed VR design.

2- Proposed Design

This section analyzes the performance of the proposed subthreshold VR. First, key specifications such as output voltage and TC are detailed. A comparative analysis of the PSRR with the reference design in [16] is then presented.

2- 1- Circuit Functional Description

The proposed VR circuit is shown in Fig. 2. To reduce power consumption, all the MOSFETs are biased in the subthreshold region. M_2 is a native nMOS transistor with an almost zero threshold voltage. Ignoring the body effect of M_2 and assuming that $V_{DS1,2} > 0.1$V, using (1), it can be driven that [16, 18]:

$$I_{D1} = \mu_{n1} C_{OX} \frac{W_1}{L_1} (m_1 - 1) V_T^2 \exp\left(\frac{V_{REF} - V_{TH1}}{m_1 V_T}\right) = I_{D2} = \mu_{n2} C_{OX} \frac{W_2}{L_2} (m_2 - 1) V_T^2 \exp\left(\frac{0 - V_{REF} - V_{TH2}}{m_2 V_T}\right) \quad (2)$$

Due to the different subthreshold slope factors of M_1 and M_2, [16] use different electron mobility values (μ_{n1} and μ_{n2}) for them, where μ_{n2} is about 1.5 times μ_{n1} [8]. Given that $I_{D1} = I_{D2}$, V_{REF} is obtained using (2). Then, by taking the derivative of V_{REF}, temperature variation on V_{REF} can be calculated. Hence, It can be written:

$$V_{REF} = m_{eq}\left((V_{TH1} - V_{TH2}) + V_T \ln\left(\frac{\mu_{n2}}{\mu_{n1}} \frac{W_2}{W_1} \frac{L_1}{L_2}\right)\right)$$
$$\frac{\delta V_{REF}}{\delta T} = m_{eq}\left(\left(\frac{\delta V_{TH1}}{\delta T} - \frac{\delta V_{TH2}}{\delta T}\right) + \frac{k}{q} \ln\left(\frac{\mu_{n2}}{\mu_{n1}} \frac{W_2}{W_1} \frac{L_1}{L_2}\right)\right) \quad (3)$$

where $m_{eq} = (m_1 \times m_2)/(m_2 + m_1)$, k is the Boltzmann constant, and q is the electron charge. It can be shown that $\left(\frac{\delta V_{TH1}}{\delta T} - \frac{\delta V_{TH2}}{\delta T}\right)$ is CTAT while the second part of the expression is PTAT. Hence, by appropriately sizing transistors M_1 and M_2, it is possible to achieve zero TC.

2- 2- PSRR Calculation

Fig. 3 shows the small-signal equivalent circuit of the proposed voltage reference (VR). Since M_1-M_4 are configured as current mirrors, they inherently possess the same bias current. Additionally, all transistor channel lengths (L_4-L_7) are equal to 1 µm. These assumptions allow us to simplify the analysis. With these assumptions, the drain-to-source

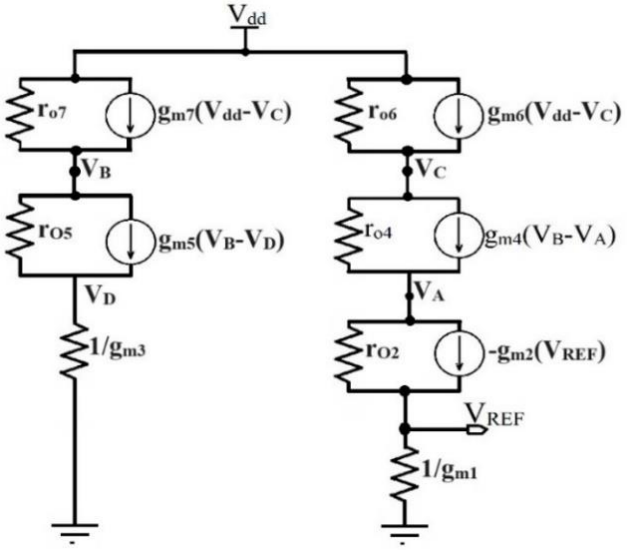


Fig. 3. The proposed VR's simplified small-signal circuit.

resistances (r_{O4}-r_{O7}) are approximately equal to r_{O4}, and the transconductances (g_{m3}-g_{m7}) are approximately equal to gm. Based on Kirchhoff's current law (KCL) to the circuit in Fig. 3 (neglecting body effects for simplicity), It can be written that :

$$\begin{aligned}
&\text{KCL } V_A: \frac{V_A-V_{REF}}{r_{o2}} - g_{m2}(V_{REF}) - g_m(V_B-V_A) + \frac{V_A-V_C}{r_{o4}}\\
&\text{KCL } V_B: \frac{V_B-V_D}{r_{o4}} + g_m(V_B-V_D) - g_m(V_{dd}-V_C) + \frac{V_B-V_{dd}}{r_{o4}}\\
&\text{KCL } V_C: \frac{V_C-V_A}{r_{o4}} + g_m(V_B-V_A) - g_m(V_{dd}-V_C) + \frac{V_C-V_{dd}}{r_o}\\
&\text{KCL } V_D: g_m(V_D) - g_m(V_B-V_D) + \frac{V_D-V_B}{r_{o4}}\\
&\text{KCL } V_{REF}: g_{m1}(V_{REF}) + g_{m2}(V_{REF}) + \frac{V_{REF}-V_A}{r_{o2}}
\end{aligned} \quad (4)$$

Using algebraic manipulations, simplifications (using the MATLAB solver), and acceptable approximations, the above equations lead to the following conclusion:

$$\begin{aligned}
\frac{V_A}{V_{dd}} &= \frac{g_m r_{oA}(3g_m r_{o4}+2)}{r_{of}g_m^3 r_{o4}^2 + g_m^2 r_{o4}^2 + 3g_m^2 r_{of} r_{o4} - 3g_m r_{o4} + 2r_{of}g_m - 2}\\
&\cong \frac{3g_m^2 r_{oA} r_{o4}}{g_m^3 r_{oA} r_{o4}^2 + g_m^2 r_{o4}^2 + 3g_m^2 r_{o4} r_{oA}} \cong \frac{3g_m^2 r_{oA} r_{o4}}{g_m^3 r_{o4}^2 r_{oA}} \cong \frac{3}{g_m r_{o4}}
\end{aligned} \quad (5)$$

where $r_{oA} = r_{o2}\left(1+\frac{g_{m2}}{g_{m1}}\right)$ On the other side, as shown in [16] it can be written as:

$$\frac{V_{REF}}{V_A} \cong \frac{1}{(g_{m1}+g_{m2})r_{o2}} \quad (6)$$

Thus, the PSSR can be derived as:

$$PSRR = \frac{v_{REF}}{v_{dd}} \cong \left[\frac{1}{(g_{m1}+g_{m2})r_{o2}}\right]\left[\frac{3}{g_m r_{o4}}\right] \quad (7)$$

As shown in (7), the PSRR is significantly improved compared to the previous work in [16]. This improvement is attributed to the term in the second part of (7).

3- Simulation of the proposed VR

The 0.18 µm CMOS technology set is used for post-layout simulation. The proposed VR layout is illustrated in Fig. 4, with an effective area of 34.7×14.8(µm)^2. The active area in [16] is equal to 1425 (µm)^2 in a standard 180 nm CMOS process. It has a lower effective area than [16], even with the higher number of transistors in the proposed VR. The proposed VR operates from 0.5V to 1.8V supply voltage. It consumes 0.72nW at T = 27°C and 0.5V of V_{dd}. Although the power consumption has increased compared to [16] due to the inclusion of new transistors and branches for improved PSRR and LS performance, the design remains a sub-nanowatt voltage reference. The sizes of the transistors are summarized in Table 1. As observed, the transistor's length in the presented work is much smaller in comparison to the previous work [16].

The proposed design does not require an additional startup circuit because the leakage current from the drain

Table 1. Sizes of transistors

Device	Value	Device	Value
M_1	10.4µm/6µm	M_3	2µm/2µm
M_2	1µm/6µm	M_4, M_5, M_6, M_7	15µm/1µm

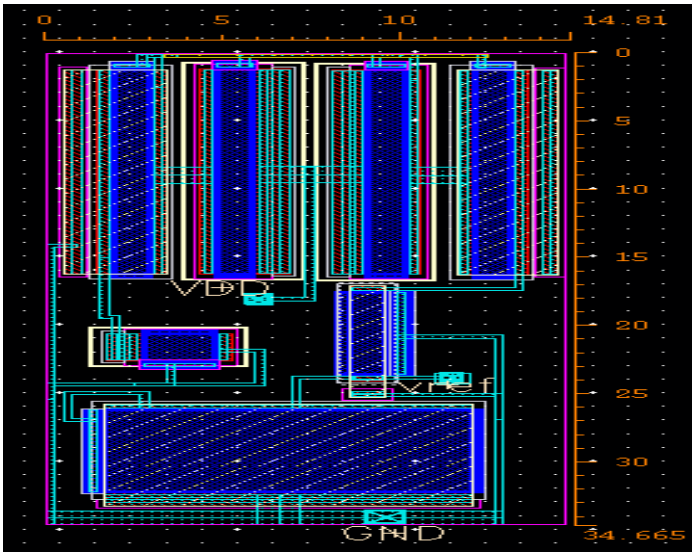


Fig. 4. Proposed VR layout

to the bulk diode of the wide-width transistor (M_4) provides sufficient current to initiate operation in M_6. Fig. 5 illustrates the transient response of the VR during start-up using a slow 0.01V/ms supply ramp from 0V to 1V. The figure shows both the supply ramp voltage and the corresponding VR output voltage.

Fig. 6 shows V_{REF} as a function of temperature from -20°C to 130°C over the minimum and maximum operating ranges for V_{dd}. It can be observed that the V_{REF} is at about 150.3mV with a TC of 12.11ppm/°C at 0.5V of V_{dd}. The TC increases to 13.63ppm/°C at the V_{dd} of 1.8V.

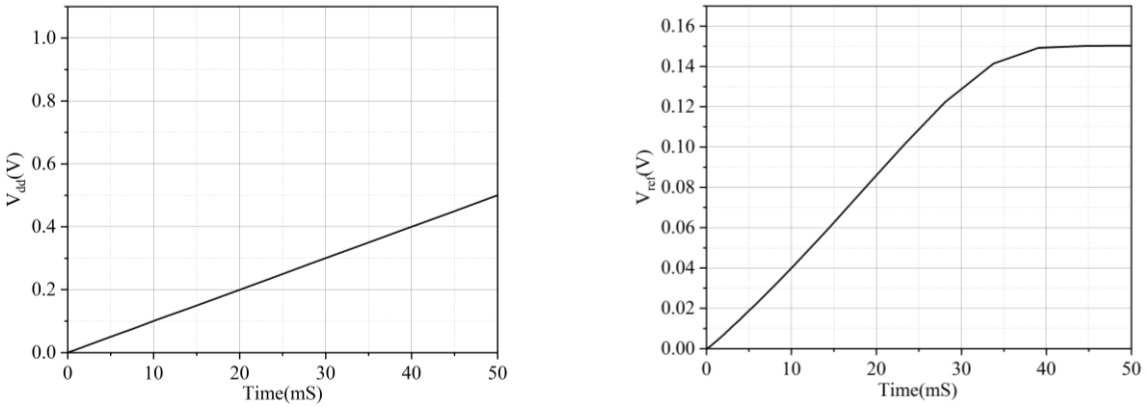
Fig. 7 shows the current consumption of the proposed voltage reference as a function of temperature, considering both the minimum and maximum supply voltage values. As observed, maximum power consumption occurs at T=130°C. It is about 0.72nW and 14.21nW, respectively, at T = 27 °C and T = 130°C with V_{dd} = 0.5V.

The output noise versus frequency at room temperature (27 °C) and V_{dd} = 0.5V is shown in Fig 8. The values of output noise are obtained as 167.34nV/√Hz, 138.35nV/√Hz, and 8.13nV/√Hz at 1 kHz, 10 kHz, and 1 MHz, respectively.

Fig. 9 shows the output voltage V_{REF} at different process corners for V_{dd} =0.5V. It is found that the TC values are obtained at 40.04 ppm/°C, 18.80 ppm/°C, 37.80ppm/°C and 47.74ppm/°C and 12.11 ppm/°C in SS, SF, FS, FF, and TT corners respectively.

Fig. 10 illustrates V_{REF} versus supply voltage at room temperature. Hence, the LS value can be calculated as follows:

$$LS\% = \frac{\Delta V_{REF}}{\Delta V_{dd}} \frac{1}{V_{REF}} \times 100 = LS\% = \frac{0.15042 - 0.15029}{(1.8 - 0.5)(0.150355)} \times 100 = 0.066\%/V \quad (8)$$



(a) (b)

Fig. 5. Transient response of the output voltage (V_{REF}) to a slow voltage ramp applied to the supply voltage (V_{dd}). a) The voltage ramp applied to V_{dd} b)Transient response of V_{ref}

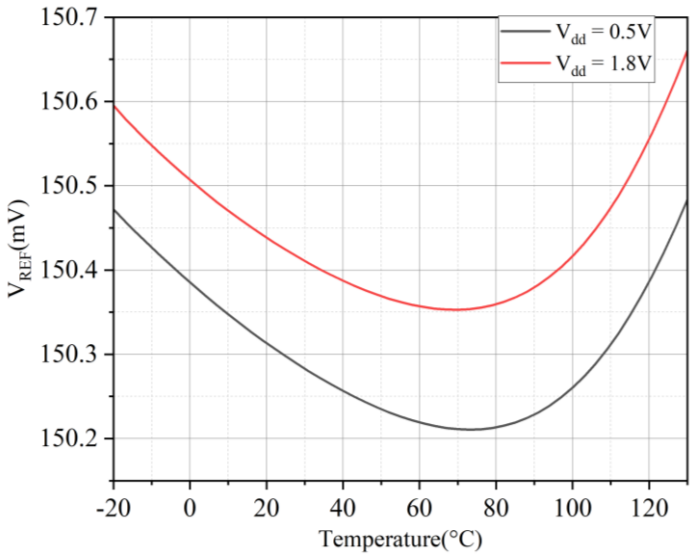


Fig. 6. Temperature variation of V_{REF} at minimum and maximum of V_{dd}

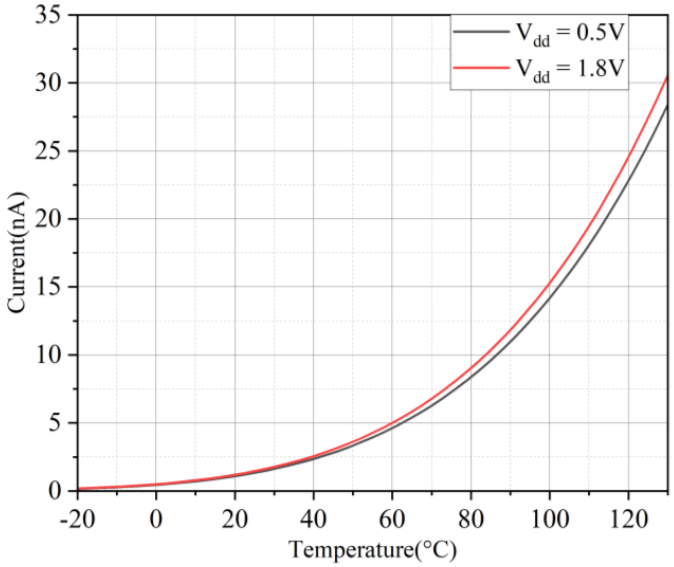


Fig. 7. Supply current consumption at different values of V_{dd}

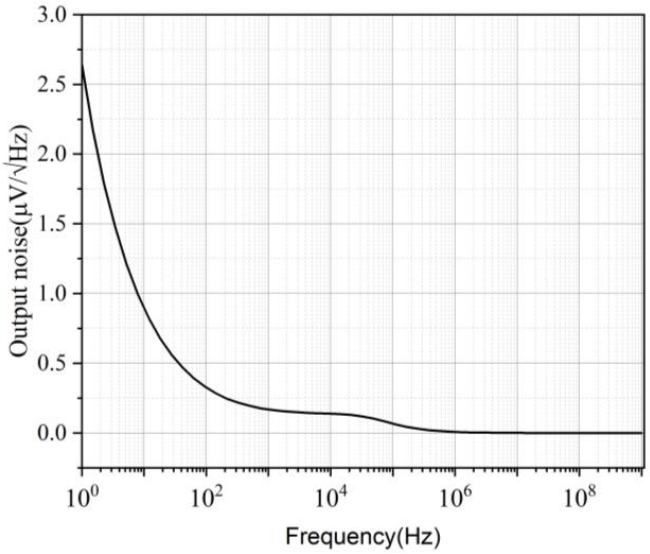


Fig. 8. Output noise for proposed VR at V_{dd} = 0.5 V.

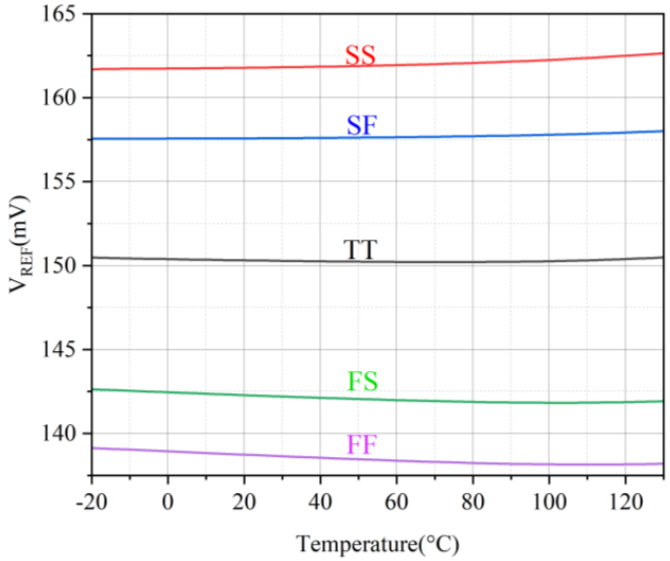


Fig. 9. V_{REF} at different process corners vs. temp at V_{dd} = 0.5V

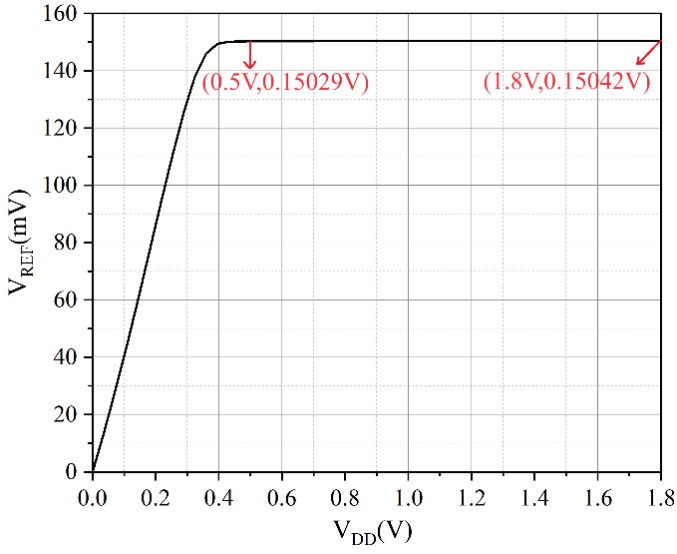


Fig. 10. Shows V_{REF} verus Vdd at T = 27°C

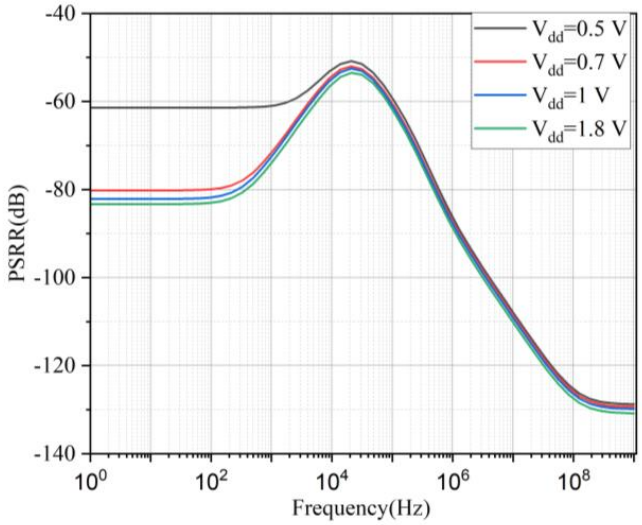


Fig. 11. PSRR vs. frequency for different supply voltages at T = 27°C

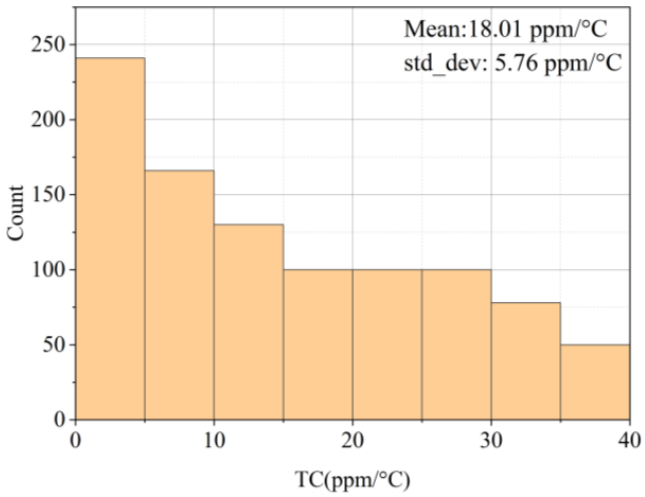


Fig. 12. Monte Carlo simulation results of 1000 runs for TC at V_{dd} = 0.5V.

The power supply voltage (V_{dd}) range being considered is from 0.5V to 1.8V while ΔV_{REF} represents the output voltage variation within this power supply voltage range.

The PSRR at 1Hz and T = 27°C is -61.4dB, -80.1dB, -82.1dB and -83.3dB at 0.5V, 0.7V, 1V and 1.8V

supply voltage, respectively, as shown in Fig. 11 where a 0.5 pF off-chip capacitance load is considered at the output node. In addition, the PSRR cut-off frequency is approximately 3.16 KHz for V_{dd} = 0.5V. As expected, the proposed voltage reference (VR) exhibits superior PSRR and LS performance compared to the previous design in [16].

Monte Carlo simulation is used to account for process variations and mismatches. Fig. 12 and Fig. 13 show the results of the Monte Carlo simulation for the TC and the nominal V_{REF} with V_{dd} = 0.5V, respectively. For the TC analysis (Fig. 12), the mean (μ) and standard deviation (σ)

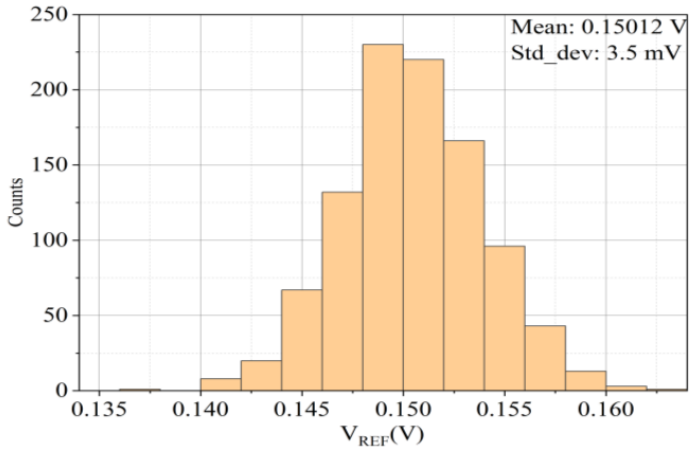


Fig. 13. Monte Carlo simulation results (1000 runs) for VREF at T = 27°C

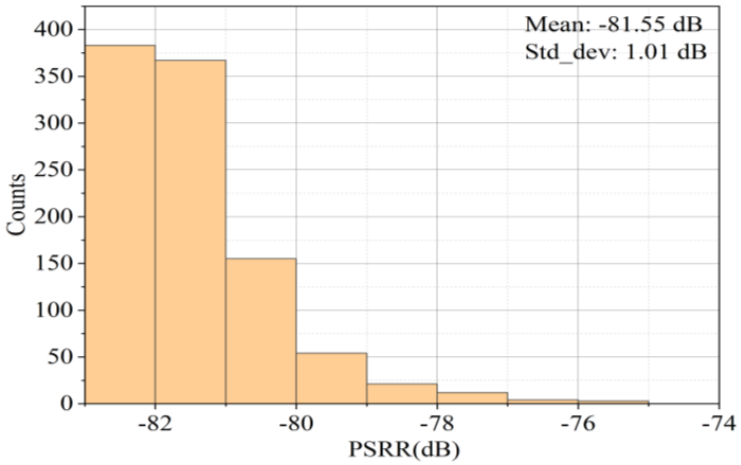


Fig. 14. Monte Carlo simulation results (1000 runs) for PSRR at V_{dd} =1V.

are 18.01 ppm/°C and 5.76 ppm/°C, respectively.

For the output voltage (V_{REF}) analysis shown in Fig. 13, the simulations yield a mean of 150.12 mV and a standard deviation of 3.5 mV. Fig. 14 then illustrates the PSRR performance. Here, the μ value for PSRR is -81.5466dB with a σ of 1.10dB, where V_{dd} = 1V. Finally, Fig. 15 presents the results for the line sensitivity. The simulations show a mean of 0.072% /V and a standard deviation of 0.009% per volt for LS.

Fig. 16 and Fig. 17 further show the temperature dependence of the PSRR and LS, respectively, at the TT corner. The figures show that the PSRR reaches approximately -80.45 dB at its worst point (T = 130°C), while the LS reaches approximately 88.86 × 10-³ ٪/V at T = ١٣٠ °C.

Fig. 18, Fig. 19, and Fig. 20 show the PSRR, LS, and V_{REF} of the proposed VR under different process corners and temperature conditions where -20°C and 130°C are used for the cold and hot temperature simulations respectively. The figures reveal that the proposed VR maintains a PSRR of -64.21 dB and exhibits a maximum LS of approximately 0.427 %/V under these different conditions. Fig. 20 also shows that the maximum and minimum values of V_{REF} are

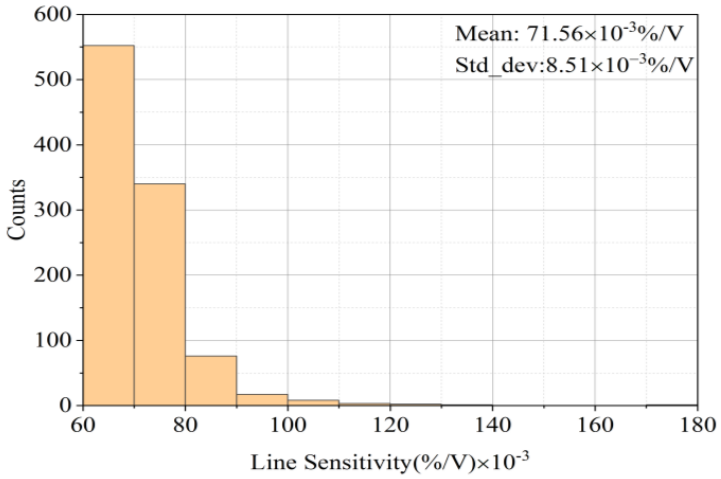


Fig. 15. Monte Carlo simulation results (1000 runs) for the line sensitivity (LS).

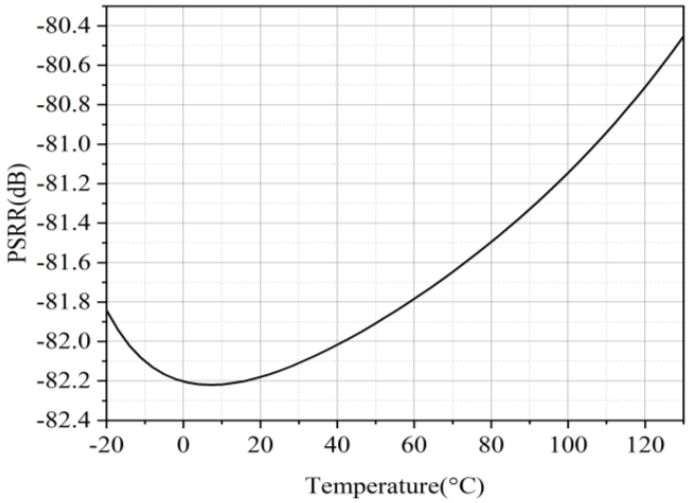


Fig. 16. Temperature dependence of the PSRR for Vdd = 1V.

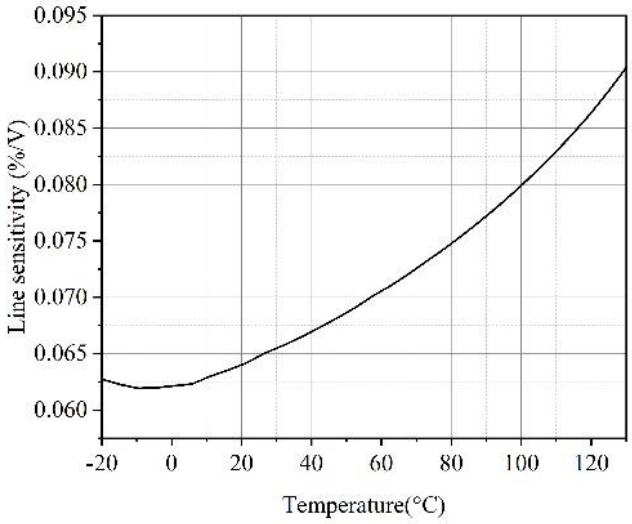


Fig. 17. Temperature dependence of the Line sensitivity.

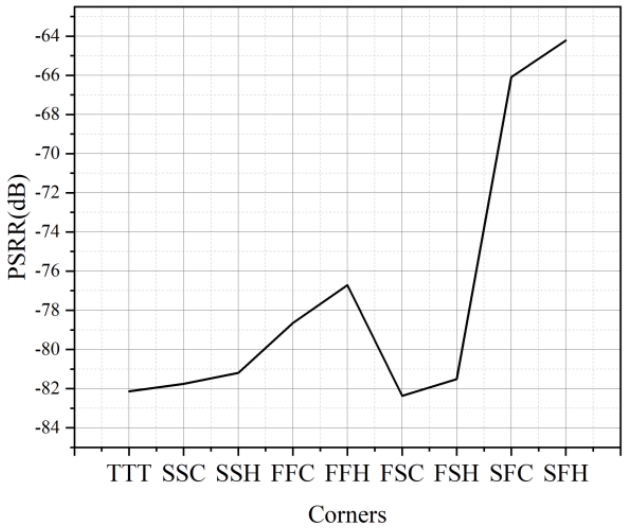


Fig. 18. PSRR in different process corners at cold and hot temperatures at V_{dd} = 1V.

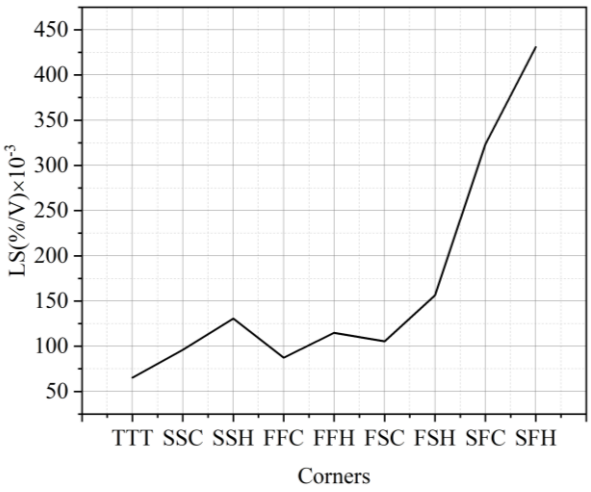


Fig. 19. Line sensitivity in different process corners at cold and hot temperatures.

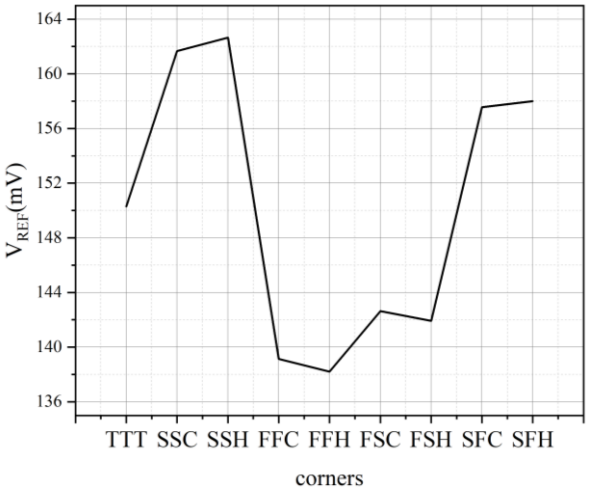


Fig. 20. Reference voltage in different process corners at cold and hot temperatures.

162.65 mV at the SSH corner and 138.2 mV at the FFH corner.

Table 2 summarizes the main characteristics of the proposed VR and presents a comparative analysis with existing literature. As expected, the proposed VR achieves good line sensitivity and high PSRR, indicating

a high degree of independence from supply voltage variations. It is important to note that the proposed design operates at a lower supply voltage (0.5V) compared to the references listed in the table. Furthermore, Table 2 reveals that the proposed VR has a lower power consumption and higher PSRR compared to the previous work presented in [8]. Also, in comparison with [3] and [13], the proposed VR has improved PSRR and lower power consumption. This advantage is due to the use of the self-bias current source to directly drive the diode-connected transistor (M_5) in our design. In contrast, the previous work uses an additional branch specifically to bias the pMOS diode-connected transistor. This additional branch contributes to increased power consumption compared to our proposed design.

Table 2. Performance summary and comparison

Design	[16]	[8]	[3]	[13]	This work
Year	2012	2019	2020	2023	2023
Tech(nm)	180	180	180	180	180
Sim/Fab	Fab	Fab	Sim	Sim	Sim
Operating temperature (℃)	-20~ 80	-40~125	0~120	0~120	-20~130
V_{dd} (V)	0.5~3.6	0.4~1.8	0.8~1.8	0.8~2	0.5~1.8
V_{REF} (mV)	330	151	625	332.85	150.12*
Power @T=27℃ (nW)	0.0055	1	16.2	15.6	0.72 @ $_{dd}$=0.5V
PSRR (dB) at 100Hz	-49	-79	-42	-44.7	-81.55* @Vdd=1V
TC (ppm/°C)	54.1	89.8	13	21.37	18.01*
Line sensitivity (%/V)	0.04	0.015	0.59	0.5	0.072*
Trimmability	NO	Yes	NO	NO	NO
Active Area(mm^2)	0.0014	0.021	0.00067	0.024	0.0005

* From Monte Carlo Results

4- conclusion

This paper proposes a novel approach to significantly reduce the effect of power supply variations on the output voltage of a subthreshold voltage reference. The proposed design utilizes a self-current biasing technique to achieve this improvement while all transistors operate in the subthreshold region. This subthreshold operation enables both low power consumption (sub-nano-watt) and compatibility with low supply voltages. Simulations using a standard 0.18 µm CMOS process demonstrate the effectiveness of the approach. The proposed voltage reference achieves an excellent PSRR of -82.1dB while maintaining a remarkably low power consumption of only 0.72nW at room temperature and a supply voltage of 0.5V.

5- Nomenclature

T	Temperature, ℃
TC	Temperature Coefficient, ppm/℃
LS	Line Sensitivity, %/V
V_{DS}	Voltage drain-source, V
I_D	Drain Current, A
C_{ox}	Gate oxide capacitance per unit area, F/m^2
W	width, m
L	length, m
m	Slope factor
V_T	Thermal Voltage, V
V_{TH}	Threshold Voltage, V
gm	Transconductance, A/V
r_o	MOSFET output resistance, Ω
μ_n	Electron mobility, $m^2/V.S$
PSRR	Power Supply Ripple Rejection
µ	Mean
σ	Standard Deviation

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