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Implementation of N-inputs Ternary to Binary Converter with Multipart division technique Based on CNTFET

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ABSTRACT: In this paper, the new structure N×M (N-Ternary inputs and M-Binary outputs) Ternary to Binary Converter based on the Carbone Nanao Tube Field Effect Transistor is presented. The Carbone Nanao Tube Field Effect Transistor (CNTFET) has special properties such as controlled threshold voltage. The aforementioned advantages related to the multi-level (more specifically Ternary) circuits and systems based on CNTFET technology have encouraged researchers to put more effort into on their design and realization in recent years. The Encoder (one input- five outputs), 3×1 multiplexer (one input – one selector-three outputs), and special Adder blocks (Full Adder and Half Adder) are base blocks that are implemented by transistor level using special properties of CNTFET transistor. In general, to implement a N-input ternary-to-binary converter, the number of inputs can be divided into two small converters, and also a ternary-to-binary converter can be designed for each input. In this paper, 2×4, 3×5, 4×7 and 5×8 Ternary to Binary converters are designed and simulated by Hospice and 32 nanometer technology. The result of the simulation is shown that the 5×8 Ternary to Binary converter has 1.89 µW DC-Power and 52 ps propagation delay. The proposed 5×8 TTBC converter is implemented by 365 CNTFET transistors and divided into two ternary to binary converters.

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1- Introduction

In the past decades, the bipolar Junction Transistor (BJT) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are the main technologies for to design of electronic circuits.

The efficiency of MOSFET technology in performance indicators of low power consumption, and high noise margin over BJT technology has led to the expansion of the design of digital electronic circuits based on MOSFET transistors.

Due to the recent advances in reducing the dimensions of MOSFET transistors in nano dimensions, important challenges such as leakage current, short channel effects, complicated manufacturing steps, and sensitivity to manufacturing process parameters have been created [1].

Therefore, the need to replace new technology seems more necessary than ever. Among the existing technologies, we can mention the double-gate FET, Strained-Si FET, FinFET, and CNTFET transistors [2, 3].

Among these technologies, CNTFET technology is a suitable candidate for designing high-frequency and low-power circuits due to its features close to MOSFET technology [4]. One of the important features of CNTFET transistors is that, unlike MOSEFT technology, both N and P transistors are the same and have similar functions, so the complexity of circuit design in this technology will be less. Among other important features in this possibility is changing the threshold voltage of transistors, this important feature makes the design of multi-level circuits much easier [5-8]. Due to the increasing volume of processes in electronic systems and the increase in the number of binary data, one of the design challenges is to reduce the space required to implement processing systems, and one solution is to use multi-level processing systems [9-13]. Compared to digital systems, these systems require less structure and communication lines, but the most important challenge of these types of systems is how to implement them using existing technologies.

In recent years, various reports have been presented on the implementation of multi-level processing systems such as three-level and four-level systems and analog systems using the capability of CNTFET transistors [10, 14-24].

The implementation of multi-level systems requires the establishment of a connection between digital systems and these systems, therefore, the implementation of data conversion systems from binary to multi-level and vice versa seems important and necessary in this regard.

In this field, various articles have been reported by researchers, for example, in Shahangian's article [24], a binary to ternary converter structure has been reported. In this report, the binary to ternary converter has been implemented using CNTFET technology.

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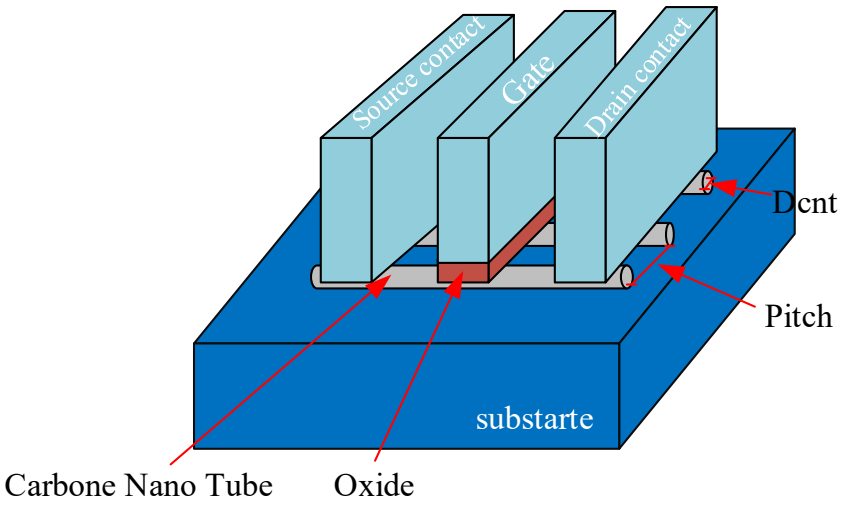

Fig. 1. The structure of CNTFET

In this article, the single-input ternary to binary converter is presented along with the necessary (basic) blocks such as decoders and types of inverters. The general technique used to implement N-digit converters is to divide the number of inputs into 2 and use a smaller converter and adder.

In this way, the final converter has better efficiency in terms of power consumption and propagation delay.

In this report, ternary to binary converter with single input-two outputs(TTBC1*2), two inputs-four outputs(TTBC2*4), three inputs-5 outputs(TTBC3*5) and 4 inputs-7 outputs(TTBC4*7), and 5 inputs - 8 outputs (TTBC5*8) is implemented at the transistor level and how to implement it is also described.

The simulation results show that these converters have good conditions compared to previous reports in terms of power consumption, propagation delay, and the number of transistors required.

In the continuation of this article, in section 2, a brief explanation of the CNTFET transistor is presented. In the third section, how to implement the proposed converters with CNTFET transistors at the transistor level is reported. In section 4, the results of the simulation of these circuits are reported in the form of graphs, waveforms and tables.

2- Structure of CNTFET

The carbon nanotube, which was discovered in 1991 by S. Iijima, is a sheet of hexagonally ordered carbon atoms that is assembled in a tube with a diameter of a few nanometers and its length can be several microns. Graphene is a single sheet of carbon atoms arranged in the well-known honeycomb structure [25].

Specially for larger and more complex circuits, the process of sizing transistors in CNTFET-based designs is less complicated than MOSFET-based designs. This is because unlike MOSFET, electrons and holes have the same mobility in the Carbone Nano Tube (μn=μp). Ballistic conductivity as well as the one-dimensional structure of CNTs reduce resistance and significantly increase velocity minimize energy loss and reduce power consumption density. In addition, removing the transistor channel also eliminates many parasitic elements.

This practical feature makes CNTFETs much more flexible for designing digital circuits than MOSFETs, and also makes the technology very suitable for designing multi-voltage threshold circuits.

The threshold voltage of a CNTFET can be calculated by Equation 1:

$$V_{th} \cong \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.D_{CNT}} \cong \frac{0.43}{D_{CNT}\,(nm)} \quad (1)$$

Here a is the atomic distance of carbon to carbon, Vp is π–π junction energy of Carbone, e electrical charge unit and DCNT is the diameter of Nano-tube Carbone.

This diameter can be calculated by the following equation in which the CNTFET threshold voltage is an inverse function of the CNT diameter:

$$V_{th} \cong \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.D_{CNT}} \cong \frac{0.43}{D_{CNT}\,(nm)} \quad (2)$$

A carbon nanotube transistor looks like a MOSFET with the same pins. In other words, the principles of operation of carbon nanotube field effect transistors are similar to current silicon transistors. Figure 1 shows the physical appearance of a carbon nanotube transistor [14]. The nanotube remains not doped in the area below the gate.

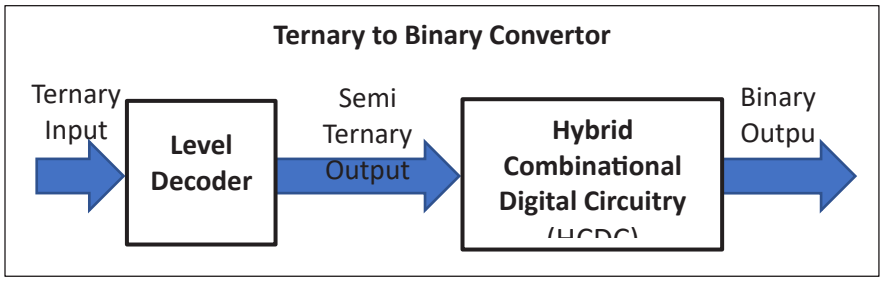

Fig. 2. Ternary to Binary Converter

The two ends of the nanotube that connect to the source and drain connections are doped areas. The voltage applied to the gate of the transistor can control the electrical conductivity of the carbon nanotube in the area below the gate by changing the electron density in the channel.

The distance between the cross-sectional centers of two adjacent carbon nanotubes below the transistor gate is called a "pitch", which significantly affects the width of the gate and the drain and source of the transistor. Interestingly, the PCNTFET and NCNTFET have the same current rate.

The gate width of the transistor can be estimated based on equation (3), in which N is the number of nanotubes under the gate, DCNT is the diameter of the nanotube and Wmin is the minimum possible width for the gate, which is determined based on lithographic constraints.

$$D_{CNT} = \frac{C_h}{\pi} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} = 0.0783\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (3)$$

3- n×m Ternary to Binary Converter (TTBC) design

The aforementioned advantages related to the multi-level (more specifically Ternary) circuits and systems based on CNTFET technology have encouraged researchers to put more effort into their design and realization in recent years. On the other hand, all available conventional digital circuits and systems are designed and operated based on a Binary base and hence it is necessary to design a suitable circuit to convert the post- processed Ternary data to its equivalent Binary counterpart. The Ternary base has three values namely 0, 1, and 2 which are equal with GND, $V_{DD}/2$, and V_{DD} voltages, respectively, while the binary base has two values, i.e. 0 and 1 corresponding with GND and V_{DD}, respectively. Unfortunately there is not a "one-to-one correspondence" between Ternary and Binary base, and thus the empty ceiling (EC) in the binary side is unavoidable and it varies depending on the number of Ternary side inputs, hence the TTBC has a heterogeneous configuration.

As it is shown at Figure 2, to convert a Ternary code to its Binary counterpart a circuit including a multi- output level decoder along with a suitable hybrid combinational digital circuit (HCDC) must be considered. The Ternary code is fed into the level decoder which generates all possible Semi Ternary variations at its output. The level decoder eliminates extra levels of the ternary code in various ways creating multiple semi Ternary outputs with voltage levels as equal as a Binary code. In other words, each Ternary input is converted to five possible outputs with a binary voltage level. The level decoder output is then processed by the hybrid combinational digital circuit (HCDC) to produce the corresponding Binary outputs.

Before dealing with TTBC decoder design procedure, let's find a way to calculate appropriate relationship between number of decoder input and output. Considering that the "n" and "m" are integer values, in order to design an "n" input / "m" output Ternary to Binary (n×m TTBC with EC=2^m-3^n) Decoder, the minimum possible "m" must be considered for each "n" for which the equation $3^n<2^m$ is valid, for example equations $3^1<2^2$, $3^2<2^4$, $3^3<2^5$, $3^4<2^7$, $3^5<2^8$ verifies the 1×2 (EC=1), 2×4 (EC=7), 3×5 (EC=5), 4×7 (EC=47) and 5×8 (EC=13) TTBC Decoders. The functionality of the n×m TTBC decoder is described in the following sub-sections starting from n=1 and it will be tried to find a general scheme for designing extended decoders.

It is worth noting that the general design rule for implementing binary outputs of 3×2^n TTBC decoder is to consider all available decoder outputs for each Ternary input (T_0, T_1, …) which is provided in Table 1 and then design the transistor level circuit of each output accordingly. The following subsections discuss different ternary to binary converters with emphasis on this general design rule.

3- 1- 1×2 Ternary to Binary converter design

As mentioned earlier, in general, it is necessary to use a Ternary to Binary converter (TTBC) when dealing with Ternary circuits. The truth table of the TTBC level decoder block is shown in Table 1. According to this table in each mode, only one of the outputs T_{i-0}, T_{i-1}, T_{i-2} is active. For example, considering T_i input equal to 1, only T_{i-1} output is active while it is zero for all other modes. Although three outputs seem to be enough for 1×2 TTBC, in fact this circuit has 5 outputs some of which are used along with the T_i input to control the transistor gates of the converter realized at the transistor level.

Table 1. single input Ternary to Binary (TTB) level decoder truth table

Ternary Input T_i		Semi Ternary Outputs									
		PTI=T_{i-2-b}		T_{i-1-b}		T_{i-2}		T_{i-1}		NTI=T_{i-0}	
0	GND	2	VDD	2	VDD	0	GND	0	GND	2	VDD
1	VDD/2	2	VDD	0	GND	0	GND	2	VDD	0	GND
2	VDD	0	GND	2	VDD	2	VDD	0	GND	0	GND

Table 2. All possible cases of the 1×2 Ternary to Binary (TTBC) decoder

Single digit Ternary Input		**Outputs (Binary)**			
		B_1		**B_0**	
0	GND	0	GND	0	GND
1	VDD/2	0	GND	1	VDD
2	VDD	1	VDD	0	GND

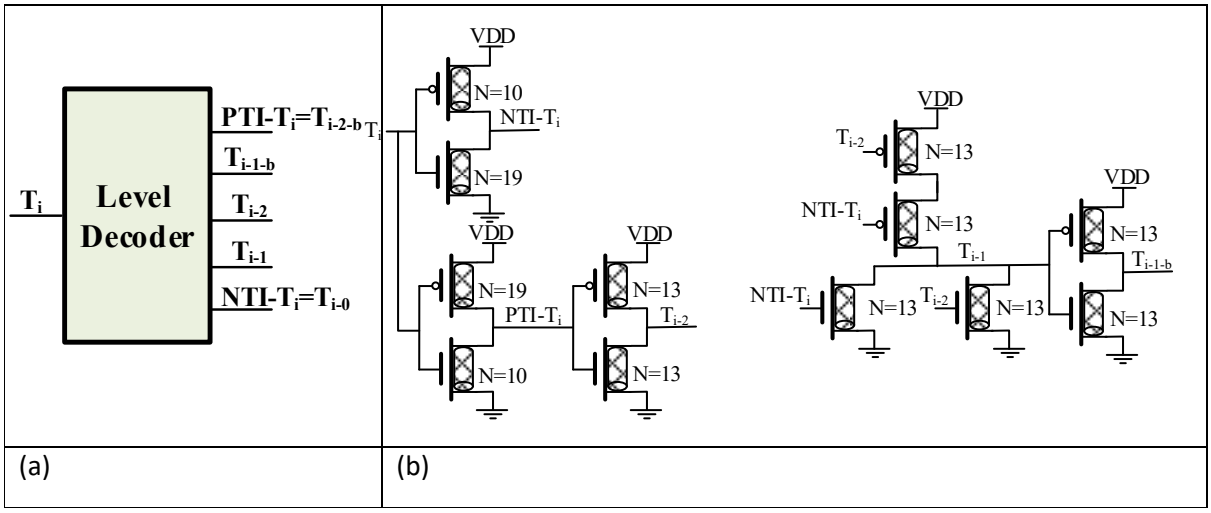

Fig. 3. Single input Ternary to Binary (TTBC) level decoder (a) Block (b) transistor level implementation

For an n×m TTBC, considering Ternary input T_i where 0£i<n, T_{i-j} is the semi-Ternary intermediate signals corresponding to the level decoder outputs where j=0, 1, and 2 depending on the value of T_i. Meanwhile, T_{i-1-b} and T_{i-2-b} which are the complement values of T_{i-1} and T_{i-2}, respectively are also required. Hence in overall for an n×m TTBC, 5×n semi Ternary intermediate signals are generated by the level decoder for further usage of the final hybrid combinational digital stage to realize the required Binary outputs, i.e. B_k where 0£k<m.

For example, for a 2×3 TTB converter, T_0 and T_1 are the Ternary inputs. T_{0-0}, T_{0-1}, T_{0-2}, T_{0-1-b}, T_{0-2-b}, T_{1-0}, T_{1-1}, T_{1-2}, T_{1-1-b}, and T_{1-2-b} are 10 outputs of the level decoder blocks which are used to create final Binary values, i.e. B_0, B_1 and B_2.

As it is shown at Table 1 the level decoder input has three levels, i.e. 0 (GND), 1 (VDD/2), and 2 (VDD) while all its semi Ternary outputs have two levels, i.e. 0 (GND) and 2 (VDD).

To design a single-input ternary to binary converter, two binary outputs are required. All possible modes are shown in Table 2. Figure 3 (b) shows the circuit structure of a 1×2 converter at the transistor level.

Table 3. 2×4 Ternary to Binary Converter (TTBC)

Ternary Inputs						Binary Outputs					
	T_1		T_0		B_3		B_2		B_1		B_0
0	GND	0	GND	0	GND	0	GND	0	GND	0	GND
0	GND	1	VDD/2	0	GND	0	GND	0	GND	1	VDD
0	GND	2	VDD	0	GND	0	GND	1	VDD	0	GND
1	VDD/2	0	GND	0	GND	0	GND	1	VDD	1	VDD
1	VDD/2	1	VDD/2	0	GND	1	VDD	0	GND	0	GND
1	VDD/2	2	VDD	0	GND	1	VDD	0	GND	1	VDD
2	VDD	0	GND	0	GND	1	VDD	1	VDD	0	GND
2	VDD	1	VDD/2	0	GND	1	VDD	1	VDD	1	VDD
2	VDD	2	VDD	1	VDD	0	GND	0	GND	0	GND

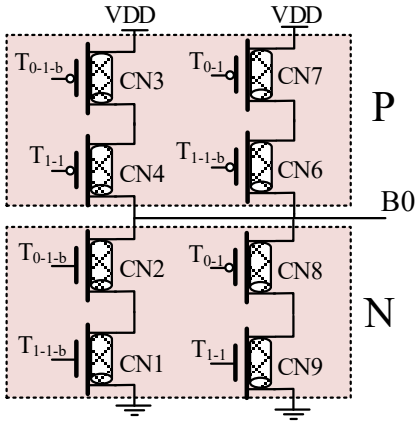

Fig. 4. Transistor level implementation of B0 output related to the two input Ternary to Binary (TTBC) decoder.

Note that mode 1 for binary outputs is the same as the V_{DD} voltage level. To obtain output B_0, according to the TTBC level decoder table, output T_{i-1} is the same as output B_0, and output B_1 is equal to T_{i-2} and hence no extra circuit is required for 1×2 converter realization.

3- 2- 2×4 Ternary to Binary converter design

Four binary outputs are required for a Ternary-to-Binary converter with two Ternary inputs. In other words, according to Table 3, the number of possible modes is 9 and in order to cover 9 modes, 4 binary outputs must be considered.

Binary outputs, namely B_3, B_2, B_1, and B_0 are designed considering the semi ternary outputs (T_{0-0}, T_{0-1}, T_{0-2}, T_{0-1-b}, T_{0-2-b}, T_{1-0}, T_{1-1}, T_{1-2}, T_{1-1-b}, and T_{1-2-b}) of the level decoders with inputs T_0 and T_1 as exhibited at Figure 3.

The transistor level circuit realization of output B0 is shown in Figure 4. In this structure, P and N networks are considered to produce 1 and 0 binary outputs. For output state 1, P network, which contains P type transistors, is activated, and for output state 0, network N, which contains N type transistors, is activated. In the same way as the CMOS digital circuit design techniques, when one network is active, the other network must be deactivated.

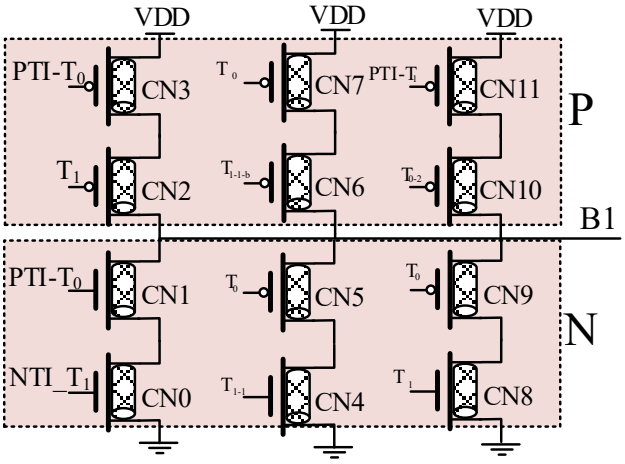

Fig. 5. Transistor level implementation of B1 output related to the two input Ternary to Binary (TTBC) decoder.

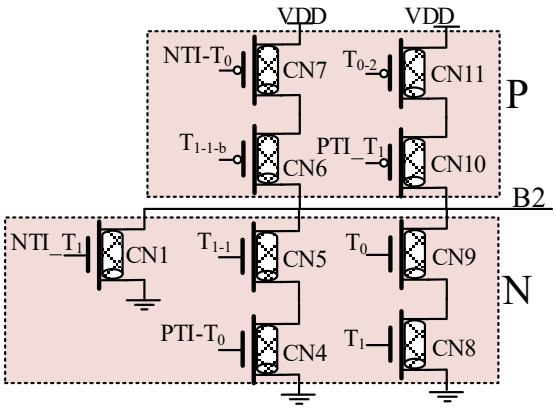

Fig. 6. Transistor level implementation of B2 output related to the two input Ternary to Binary (TTBC) decoder.

According to the truth table, in cases the input T1 is equal to 0 and 2, the output B0 depends on the input state T0. Note that in this condition the output is zero only in the case that B0 = 1, so the signals T1-1-b and T0-1-b can be used with two N-type transistors (CN1, CN2) in series as shown in Figure 4 to connect the output to ground. To connect the output to VDD in these conditions, two series transistors can be used, the gates of which are controlled by signals T1-1 and T0-1-b. For T1 = 1 and T0 = 1, the output must be connected to ground. For this purpose, two series transistors (CN3, CN4) are used, the gates of which are controlled by T0-1, T1-1 signals. For T1 = 1 and T0 = 0 and 2 the output must be connected to the VDD, two series transistors are used to implement these conditions, the gates of which are controlled by T0-1, T1-1-b signals. The full circuit of this output, namely B0 is shown in Figure 4. Regardless of the number of transistors required for the level decoder block, the hybrid combinational digital circuit requires 8 transistors to generate output B0.

To produce output B1, consider that it is zero when T1=1 and T0 = 0 and 1. For this purpose, we use two N-type transistors, the gates of which are controlled by PTI-T0 and NTI-T1 signals. For the cases T1 = 0, T0 = 2, two P-type transistors are used which are controlled by PTI-T1 and T0 control signals. The complete circuit of the output B1 is shown in Figure 5. 12 transistors are required to implement output B1.

To design the hybrid combinational digital circuit of output B2 according to the truth table (Table 3), when T1=0 the output B2 is zero, so using transistor CN0 whose gate is controlled by NTI-T1 signal, it can be guaranteed for T1 = 0 that the output B2 is connected to ground via transistor CN0. According to Table (3), for T1 = 1, output B2 must be connected to ground for T2 = 0. This is done by CN1 and CN2 transistors connected in series (Figure 6) while their gates are controlled by signals T1-1 and NTI-T0, respectively, and also if T1 = 1 for T1 being 1 or 2, the output must be connected to VDD. To implement this condition, CN3 and CN4 P type transistors are connected in series and the gate of these transistors is controlled by T11-b and NTI-T0 signals, respectively.

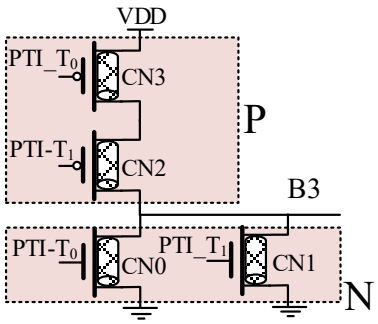

Fig. 7. Transistor level implementation of B3 output related to the two input Ternary to Binary (TTBC) decoder.

Table 4. Number of transistors required for level decoder and hybrid combinational digital circuits of the 2 to 4 converter

Blocks	Level Decoder	Hybrid Combinational Digital Circuits				TTBC2*4
		B0	B1	B2	B3	
Number of Transistor	24	8	12	9	4	**57**

Next, considering the truth table (Table 3) to design the transistor level circuit of B2, it is obvious that for T1 = 2 and T0 = 2, the output B2 should be grounded. This is realized by the N network, which includes CN5, 6 series transistors, whose gates are controlled by T1 and T2 signals. Since in this network the transistor CN6 should be activated only for state T0 = 2 hence n should be adjusted to n = 8. CN7, 8 transistors connect node B2 to VDD for T1 = 2, T0 = 0 and 1. The gates of these transistors are controlled by PTI-T1 and T0 signals, and to ensure aforementioned condition, transistor CN8 should be set to n = 19 to be activated for T0 = 0 and 1.

To describe how to implement circuit B3 according to the truth table (Table 3), we recognize that when T1= 0, 1 and T0 = 0, 1 the output B3 must be connected to ground. This is done using parallel transistors CN0, 1 and for this purpose, the gate of these transistors are controlled by PTI-T0, PTI-T1 signals. The only case where the output is connected to VDD is when T0=T1=2, so the gate of two CN2, 3 series transistors are connected to PTI-T0, PTI-T1 signals. The transistor-level circuit of output B3 is shown in Figure 7.

3- 3- 3×5 Ternary to Binary converter design

Along with the basic level decoder and hybrid combinational digital circuit (HCDC) blocks, here a multiplexer block is also required for implementing the 3 to 5 converter. The structure of the multiplexer and its function is such that when the selector signal S is equal to 0, the input I0 is connected to the output Y0, and for the selector signal being S = 1, the input I1 is connected to the output and when the signal is S = 2, I2 input is connected to output. The transistor-level circuit and the 3 to 1 multiplexer truth table are shown in Figure 8.

Figure 9 shows the block structure of a 3 to 5 TTB converter. This structure uses three hybrid combinational digital blocks and a 3×1 Ternary multiplexer. The selector of the multiplexer, namely S, is connected to T2, so for T2 = 0 the intermediate output of Bi0 is connected to Bi, and thus the intermediate outputs Bi1 and Bi2 are connected to the Bi output for T2 = 1 and T2 = 2, respectively.

According to the truth table of the 3 to 5 Ternary to binary converter, for three Ternary inputs T0, T1, and T2, there are 27 possible modes for outputs B0 to B4. To implement the B0 output, it is considered in three parts depending on the value of T2.

For T2=0, B0 is equal with B00. Considering this condition the first 9 out of the 27 states, i.e. B00, are according to the truth table of the 2 to 4 Ternary to binary converter, so the transistor level circuit of these 9 states is according to the circuit provided at Figure 4. The second 9 cases, i.e. B01 where input is T2=1, is the inverse of B00, so just an inverter is needed to produce B01 from B00. It is clear that according to Table 5, the third 9 cases, i.e. B02 where input is T2=2 is equal to B00 and hence the output of the same circuit can be reused.

To implement B1 output, it is necessary to design hybrid combinational digital circuits that create intermediate outputs B10, B11, and B12. According to Table 5, the first 9 cases, i.e. B10 where T2 = 0, it is equal to the B1output of 2 to 4 TTB converter, so using the transistor level circuit of Figure 5, B10 output of 3 to 5 TTB converter can be produced. On the other hand, the third 9 cases, i.e. B12 where T2 = 2, is exactly the inverse of the B10 output. So B12 will be produced by inverting the B10output. The hybrid combinational digital circuit of Figure 10 is used to implement B11output.

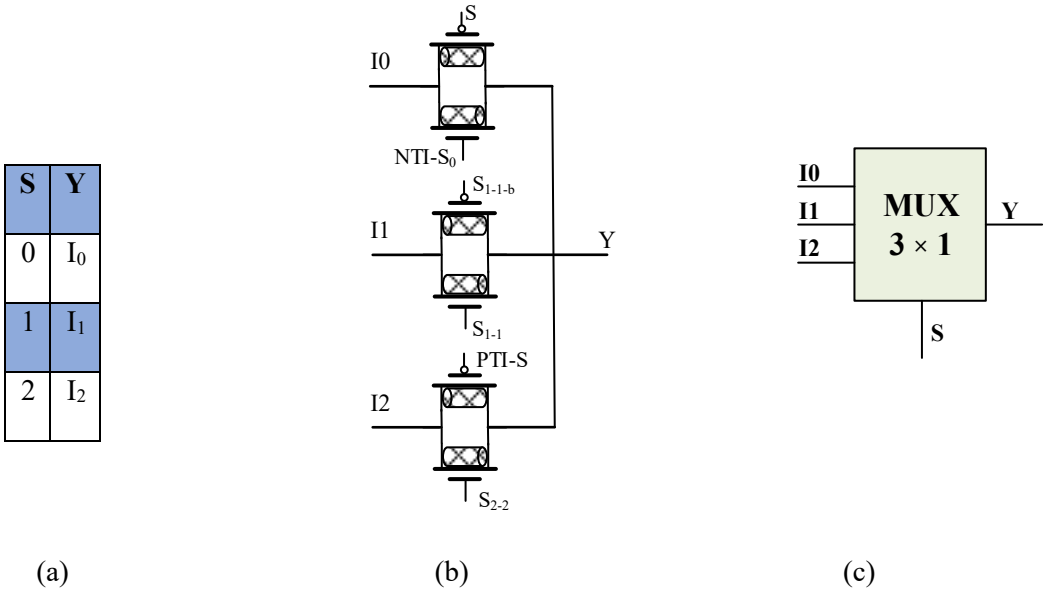

Fig. 8. (a) Truth Table, (b) Transistor level circuit and (c) Block diagram of 3×1 Ternary multiplexer

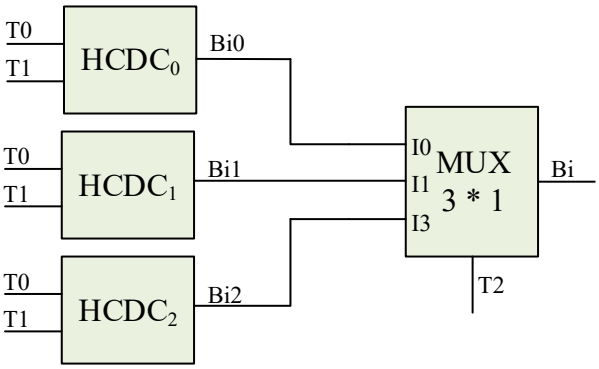

Fig. 9. Block diagram of 3 to 5 Ternary converter outputs (i = 0,1,…, 4)

Table 5. All possible modes of 3 to 5 Ternary to Binary converter

Inputs				Outputs (Binary)				
T_2	**T_1**	**T_0**	**DEC**	B_4	B_3	B_2	B_1	B_0
0	**0**	**0**	**0**	0	0	0	0	0
0	**0**	**1**	**1**	0	0	0	0	1
0	**0**	**2**	**2**	0	0	0	1	0
0	**1**	**0**	**3**	0	0	0	1	1

0	**1**	**1**	**4**	B40	0	B30	0	B20	1	B10	0	B00	0
0	**1**	**2**	**5**		0		0		1		0		1
0	**2**	**0**	**6**		0		0		1		1		0
0	**2**	**1**	**7**		0		0		1		1		1
0	**2**	**2**	**8**		0		1		0		0		0
1	**0**	**0**	**9**		0		1		0		0		1
1	**0**	**1**	**10**		0		1		0		1		0
1	**0**	**2**	**11**		0		1		0		1		1
1	**1**	**0**	**12**		0		1		1		0		0
1	**1**	**1**	**13**	B41	0	B31	1	B21	1	B11	0	B01	1
1	**1**	**2**	**14**		0		1		1		1		0
1	**2**	**0**	**15**		0		1		1		1		1
1	**2**	**1**	**16**		1		0		0		0		0
1	**2**	**2**	**17**		1		0		0		0		1
2	**0**	**0**	**18**		1		0		0		1		0
2	**0**	**1**	**19**		1		0		0		1		1
2	**0**	**2**	**20**		1		0		1		0		0
2	**1**	**0**	**21**	B42	1	B32	0	B22	1	B12	0	B02	1
2	**1**	**1**	**22**		1		0		1		1		0
2	**1**	**2**	**23**		1		0		1		1		1
2	**2**	**0**	**24**		1		1		0		0		0
2	**2**	**1**	**25**		1		1		0		0		1
2	**2**	**2**	**26**		1		1		0		1		0

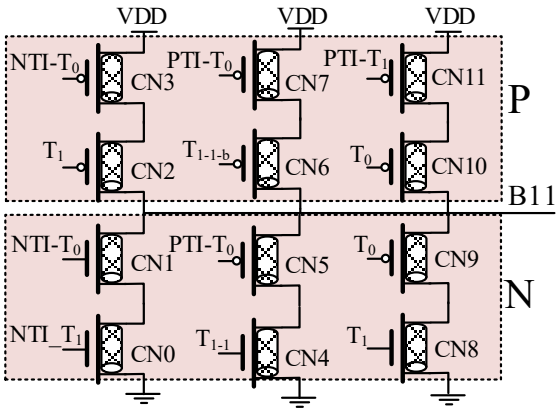

Fig. 10. transistor level circuit of B11 output for a three-input TTB converter

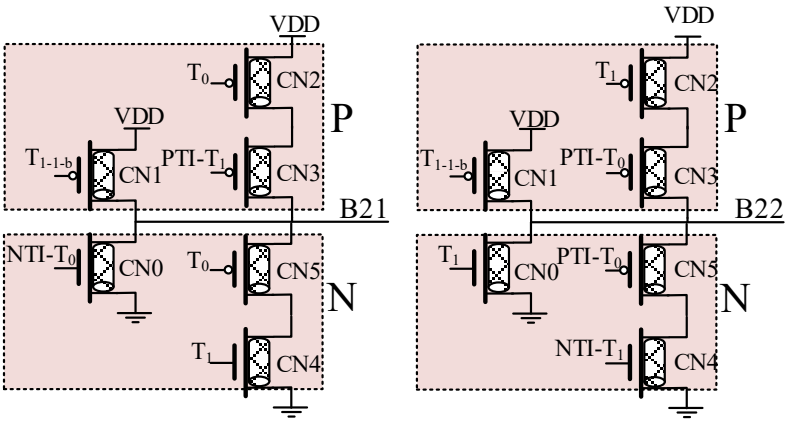

Fig. 11. Transistor level circuit of B22 and B21 outputs for the three-input TTB converter

To implement B2 output, it is necessary to design hybrid combinational digital circuits that create intermediate outputs B20, B21, and B22. For this purpose, the circuit to generate B20 output is as shown in Figure 6, and the circuits required to produce the B21 and B22 outputs are shown in Figure 11.

To implement B3 output, it is clear from Table 5 that for the first 9 cases (T2=0) the B30output of 3 to 5 TTB converter is the same as B3 output of 2 to 4 TTB, and therefore its transistor level circuit is according to Figure 7. Transistor level circuits for the implementation of B31 and B32 outputs are shown in Figure 12.

According to the truth table of Table 5, the B4 output is zero for T2 = 0 and a logic (2) for T2 = 2. The circuit of Figure 13 is just needed to produce the B41output.

Table 6 shows the number of transistors required to implement each of the outputs and the level decoder block of the proposed 3-to-5 TTB converter.

3- 4- 4×7 Ternary to Binary converter design

The overall structure of a 4-to-7 TTB converter is shown in Figure 14. This converter has 4 inputs, namely T0. T1, T2 and T3. It includes a 2-to-4 TTB converter, a 2-to-7 TTB converter, and a 7-bit addition circuit. The 2 to 4 TTB converter block is exactly the same as the one described in section 3.2.

All the operating modes of the 2 to 7 converter are shown in Table 7. Since the decimal value of the two inputs of the 2 to 7 converter is 9 and 27, respectively, so 7 binary outputs are required to convert the two Ternary inputs T2 and T3 to their binary counterparts. According to the following equation, the binary equivalent of two T2 and T3 inputs can be calculated.

$$T_3 \times 27 + T_2 \times 9 = B_6 \times 64 + B_5 \times 32 + B_4 \times 16 + B_3 \times 8 + B_2 \times 4 + B_1 \times 2 + B_0 \times 1 \quad (4)$$

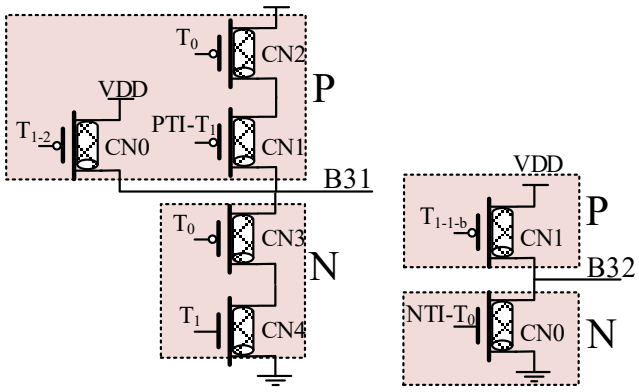

Fig. 12. Transistor level implementation of B31 and B32 outputs for three inputs Turner to Binary Converter

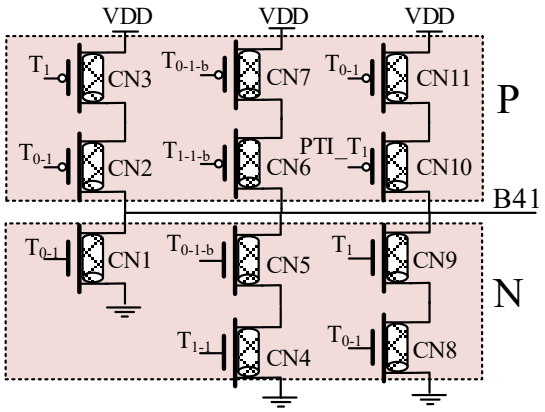

Fig. 13. three-input TTB converter B41 output transistor level implementation

Table 6. 3 to 5 TTB converter different blocks number of transistors

Blocks	Decoder	B0	B1	B2	B3	B4	**TTBC3*5**
Number of Transistor	36	16	32	27	23	9	**149**

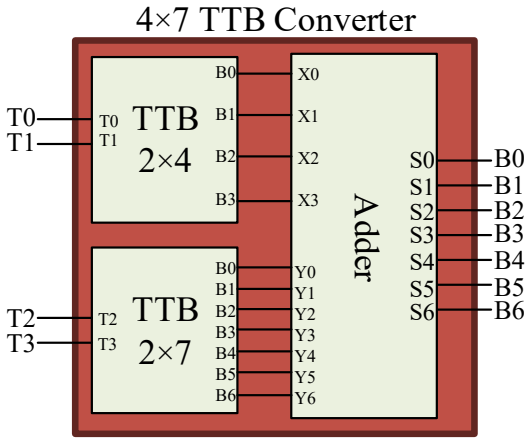

Fig. 14. Block diagram of a 4×7 TTB converter

Table 7. All possible modes for 2 to 7 TTB Converter

Inputs			Outputs (Binary)						
T_3	T_2	DEC	B_6	B_5	B_4	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0	0	0
0	1	9	0	0	0	1	0	0	1
0	2	18	0	0	1	0	0	1	0
1	0	27	0	0	1	1	0	1	1
1	1	36	0	1	0	0	1	0	0
1	2	45	0	1	0	1	1	0	1
2	0	54	0	1	1	0	1	1	0
2	1	63	0	1	1	1	1	1	1
2	2	72	1	0	0	1	0	0	0

Table 7 shows all 9 possible modes for the 2 to 7 TTB converter. The output conditions of B4 are exactly the same as B1, and also the output of B5 is exactly the same as B2, so there is no need for a separate circuit to produce B4 and B5. Comparing this table with the 2 to 4 TTB converter's truth table (Table 3), it is observed that the transistor level circuits of the outputs B0, B1, B2, B6 correspond to the circuits of Figures 4, 5, 6, and 7, respectively. Under these conditions, the transistor level implementation of the only remaining output i.e. B3 is also shown in Figure 15. Table 8 lists the number of transistors required to implement each one of the outputs.

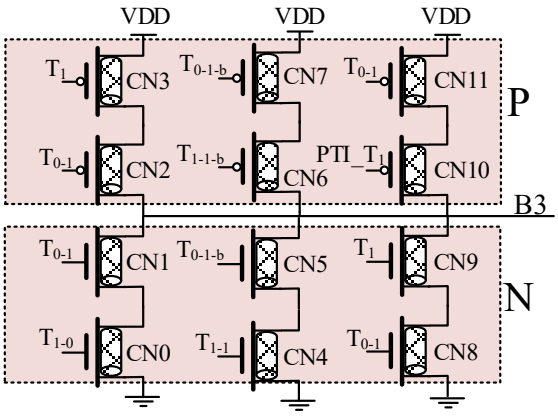

Fig 15. Transistor level implementation of Output B3 of 4 Inputs TTB Converter

Table 8. Number of transistors required for different 2-to-7 TTB converter blocks

The Blocks of TTBC2*7	B0	B1	B2	B3	B4	B5	B6	Decoder	**TTBC2*7**
Number of Transistor	8	12	9	12	0	0	4	24	**69**

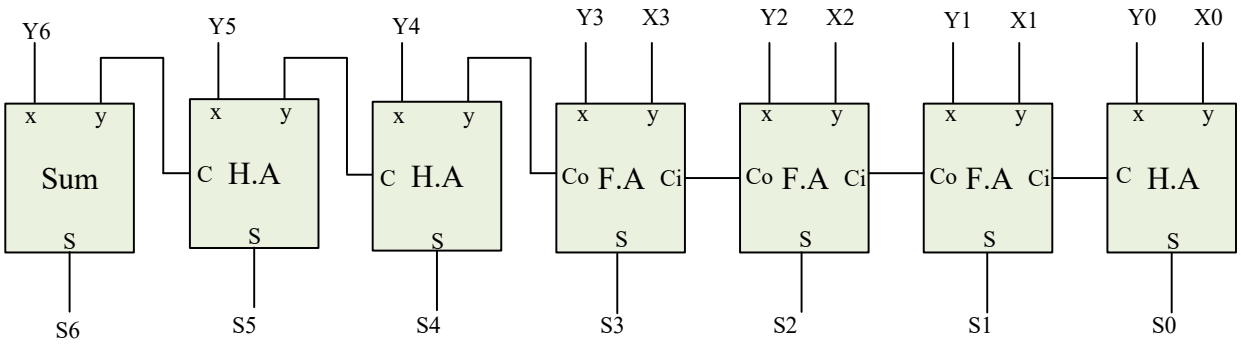

Fig. 16. Addition block diagram used in a 4 to 7 TTB converter

To implement the adder block required to implement the 4 to 7 TTB converter, given that one of the inputs is 4-bit and the other is 7-bit, the structure of Figure 16 is used. This structure requires 3 half-adders and three full adders and one half-adder block that only produces sum output. The transistor level of the half-adder and full-adder blocks are shown in Figure 17 [24].

3- 5- 5×8 Ternary to Binary converter design

The block diagram according to Figure 18 is used to implement the 5 to 8 TTB converter. In this structure, two 2 to 4 and 3 to 8 TTB converters are used along with an 8-bit adder block. The transistor level implementation of the 2 to 4 converter is the same as discussed in section 3-2. To design the 3 to 8 TTB converter according to the truth table shown in the Table 9, an algorithm similar to the one described in section 3-4 is used.

Equation 5 shows the logical relationship between Bi outputs and Tj inputs (where 0£i£7 and 0£j£4).

$$T_4 \times 81 + T_3 \times 27 + T_2 \times 9 = B_7 \times 128 + B_6 \times 64 + B_5 \times 32 + B_4 \times 16 + B_3 \times 8 + B_2 \times 4 + B_1 \times 2 + B_0 \times 1 \quad (5)$$

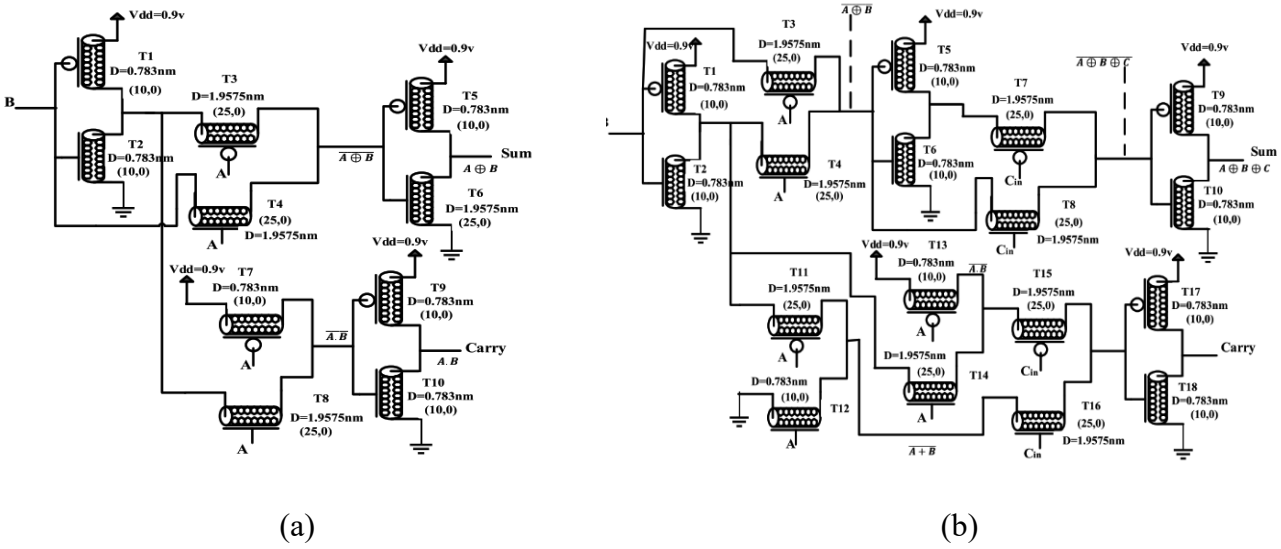

Fig. 17. Surface circuits of half-collector and all-collector transistors [24]

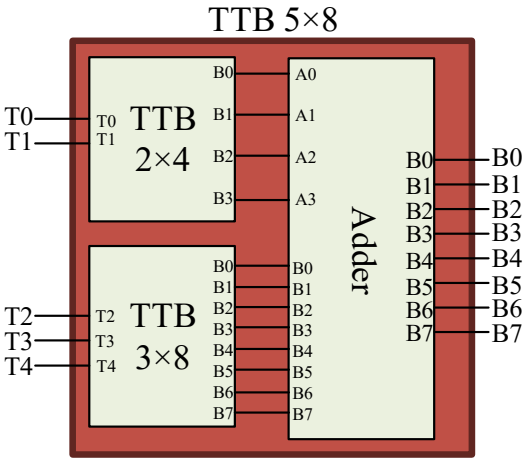

Fig. 18. Block diagram of 5×8 TTB Converter

Considering that the 3 to 8 TTB Converter inputs T2, T3, T4 have Weighted values of 9, 27, 81, respectively, so the output of this converter according to Table 9 includes 8 outputs, namely B0, B1, …, and B7. To implement each one of these outputs, along with the basic level decoder, a 3-to-1 multiplexer and three hybrid combinational digital blocks are required. The inputs of each multiplexer are Bi0, Bi1, Bi2. These intermediate outputs are produced according to the truth table. The circuits required for the implementation of each of these outputs, i.e. Bi0, Bi1, Bi2, depend on the inputs T2 and T3. In other words, if we divide the table into 3 parts, the first 9 states show the state Bi0, the second 9 states is considered Bi1, and the third 9 states is Bi2.

According to the truth table (Table 9) to implement the transistor level circuit of the outputs B0, B1 and B2, comparing this table with the truth table of the 3 to 5 TTB converter (Table 3), we find that the circuit required to obtain the outputs B0, B1 and B2 of this converter are the same as are required for outputs B0, B1 and B2 of 3 to 8 TTB converter.

The third 9 states of output B3, i.e. B32 output (Table 9) is the same as the B02output, and Figure 19 shows the transistor level circuits of the middle outputs B30 and B31.

To create output B4, considering that the B40 and B42 outputs are equal to the B10 output, then there is no need to design a separate circuit. The intermediate output B41 can be obtained using the circuit of Figure 20. The output of B41 is similar in the case of T3 = 2 and T3 = 1, so by combining them, the circuit can be designed more easily. The same conditions apply to the intermediate output B42 and its circuit is shown in Figure 20.

Table 9. All possible modes for 3 to 8 TTB converter

Inputs (Ternary)			Outputs (Binary)													
T_2	T_3	T_4	B_0		B_1		B_2		B_3		B_4		B_5		B_6		B_7
0	**0**	**0**	0		0		0		0		0		0		0		0
1	**0**	**0**	1		0		0		1		0		0		0		0
2	**0**	**0**	0		1		0		0		1		0		0		0
0	**1**	**0**	1		1		0		1		1		0		0		0
1	**1**	**0**	B00	0	B10	0	B20	1	B30	0	B40	0	B50	1	B60	0	B70	0
2	**1**	**0**	1		0		1		1		0		1		0		0
0	**2**	**0**	0		1		1		0		1		1		0		0
1	**2**	**0**	1		1		1		1		1		1		0		0
2	**2**	**0**	0		0		0		1		0		0		0		0
0	**0**	**1**	1		0		0		0		1		0		0		0
1	**0**	**1**	0		1		0		1		1		0		0		0
2	**0**	**1**	1		1		0		0		0		1		0		0
0	**1**	**1**	0		0		1		1		0		1		0		0
1	**1**	**1**	B01	1	B11	0	B21	1	B31	1	B41	1	B51	1	B61	0	B71	0
2	**1**	**1**	0		1		1		1		1		1		0		0
0	**2**	**1**	1		1		1		0		0		0		0		1
1	**2**	**1**	0		0		0		0		1		0		0		1
2	**2**	**1**	1		0		0		1		1		0		0		1
0	**0**	**2**	0		1		0		0		0		1		0		1
1	**0**	**2**	1		1		0		1		0		1		0		1
2	**0**	**2**	B02	0	B12	0	B22	1	B32	1	B42	1	B52	1	B62	0	B72	1
0	**1**	**2**	1		0		1		1		1		1		0		1
1	**1**	**2**	0		1		1		0		0		0		1		1
2	**1**	**2**	1		1		1		1		0		0		1		1

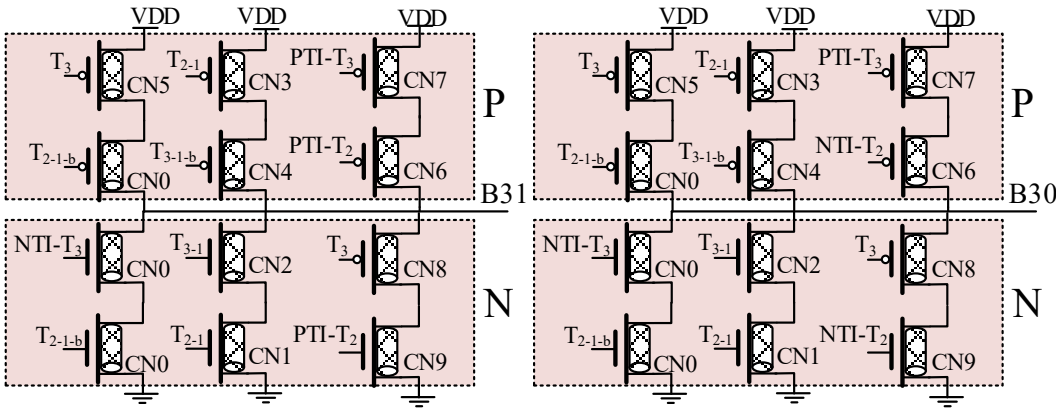

Fig. 19. Transistor level implementation of B30 and B31 Output

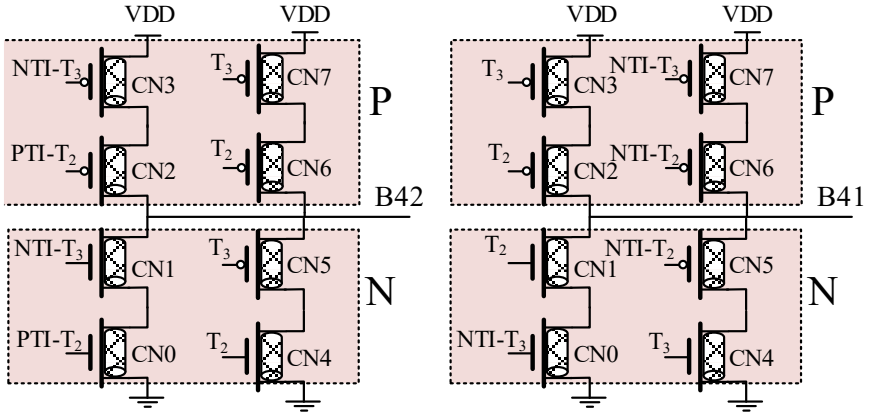

Fig. 20. Transistor level implementation of B41 and B42 Outputs

In the implementation of output B5, since the intermediate output of B50 is equal to B2 of 2×۴ TTB converter, the circuit shown at Figure 6 can be used for B50. The rest of the intermediate outputs can be obtained according to the transistor level circuits shown in the Figure 21.

To implement the transistor level circuit of B6, according to the intermediate output truth table B60=B61=0, and the intermediate output B62 is obtained from the circuit shown in the Figure 22.

The circuit in Figure 23 shows that 6 transistors are required to implement B7.

The number of transistors required for each circuit is shown separately in Table 10. The Adder block, using the structure shown in Figure 24 adds a 4 bits data with an 8 bits one, to generate the final outputs of the TTB converter. One of the advantages of using this structure is to generate the output of 2 to 4 and 3 to 8 TTB converters simultaneously. This condition increases the conversion speed. 180 transistors are required to implement this Adder.

3- 6- N-digit Ternary to Binary converter design

In general, to implement a N-digit ternary-to-binary converter, the number of inputs can be divided into two, and a ternary-to-binary converter can be designed for each input. Considering Figure 25 it should be noted that the converter outputs of the second part (TTBC2) have different weight. In this figure, N is the number of TTB converter inputs and M is the number of converter outputs.

In this structure, simultaneously with the output of B00… B0i outputs by the TTBC1 converter, the intermediate outputs of B10… B1j are also generated by the TTBC2 converter. Consequently, the final outputs of the N-digit ternary-to-binary converter is generated using a multi-bit ternary adder. The adder block also consists of half-adder and full adder blocks that add the inputs B00… B0i with B10… B1M.

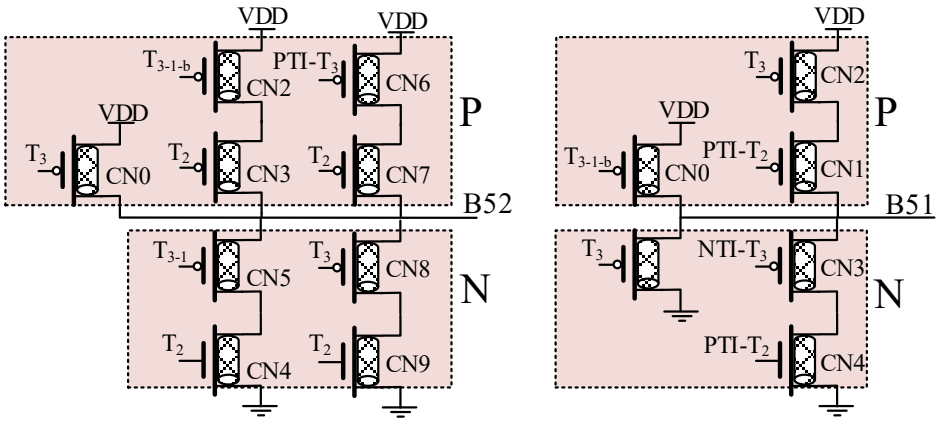

Fig. 21. Transistor level implementation of B51 and B52 outputs

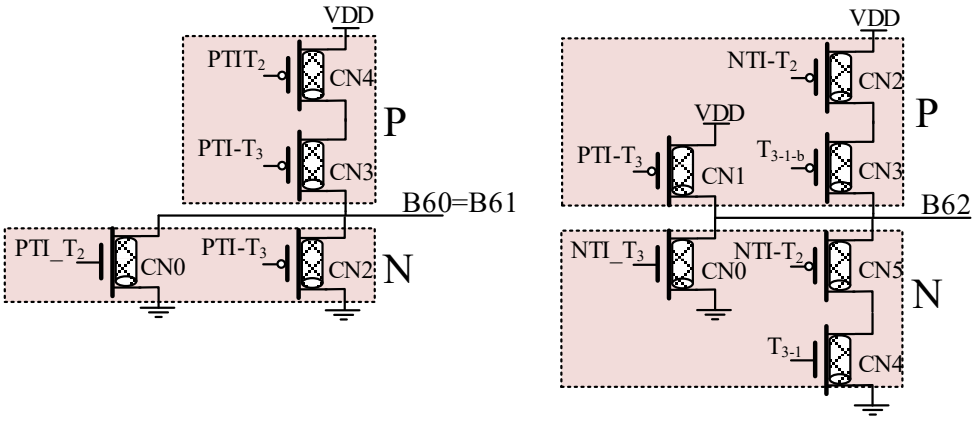

Fig. 22. transistor level implementation of B60, B61, and B62 Outputs

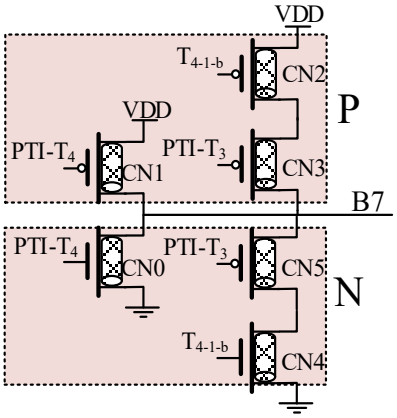

Fig. 23. Transistor level implementation of B7 output

Table 10. Number of transistors required for implementation of different sections of 3 to 8 TTB converter, including level decoder and output section, separately

3 to 8 TTB converter different parts	Level decoder	B0	B1	B2	B3	B4	B5	B6	B7	**TTBC3*8**
Number of Transistor	36	16	32	27	28	22	24	16	6	**207**

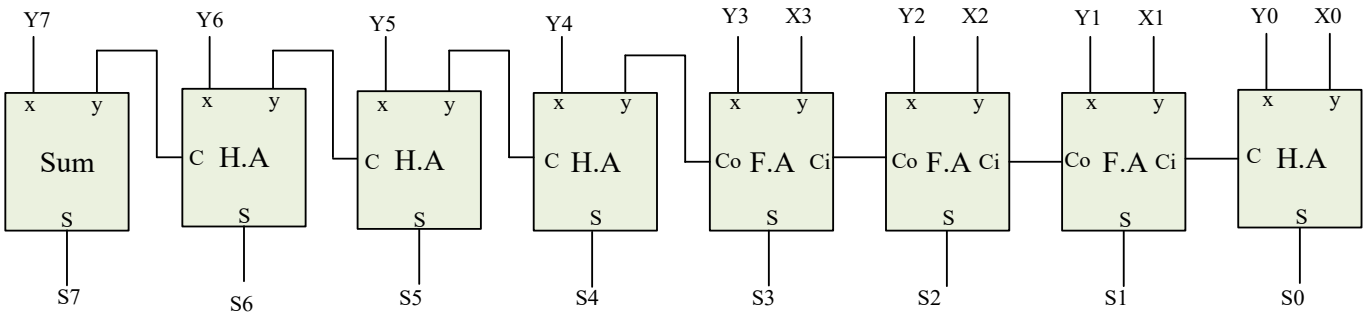

Fig. 24. Adder block diagram used in 5 to 8 TTB converter

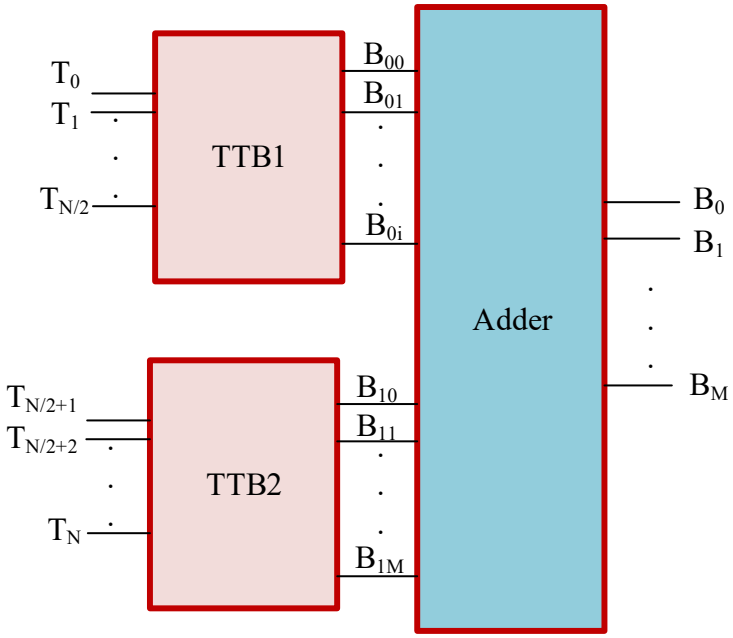

Fig. 25. N-digit TTB converter block diagram

Table 11. Parameters of CNTFET

CNT Parameters	Symbol	Typical Value
Physical channel length	Lch	32 nm
The length of doped CNT source/drain extension region	Lss	32 nm
The mean-free-path in intrinsic CNT channel	Lgeff	100 nm
The width of metal gate	Wgate	6.4
The dielectric constant of high-k top gate dielectric material(HfO2)	Kgate	16
The thickness of high-k top (planner) gate dielectric material(HfO2)	Tox	4 nm
The diameter of CNT	Dcnt	1.49 nm
The distance between the centers of two adjacent CNTs	S or Pitch	20 nm
The chirality vector of tubes	(n1,n2)	(19,0)

4- Simulation results

To test the correct operation of the proposed arithmetic circuits they are simulated at HSPICE software using 32 nm CNTFET transistor model. All of the proposed blocks have been simulated at the transistor level utilizing the power supply of 0.9 V. The results show that for all possible input cases the outputs of the proposed TTBC are correct.

This converter has 3 binary outputs for one ternary input, and the time graph of the waveform of each output compared to the input state can be seen in Figure 26. As mentioned in the circuit design section, 12 transistors are needed to implement the decoder circuit. In fact, the single-input decoder block is the same as the ternary-to-binary converter, and the outputs T0_1, T0_2 are the binary outputs of the single-input converter.

The TTBC 2×4 converter has two ternary inputs and four binary outputs. Figure 27 shows the waveforms of the outputs in all possible states for this converter, for example, at time 17 ns for the input state "11", the output of the converter is B = "0100".

The results of the simulation of TTBC2×4 are shown in Table 12. The simulation results compared to reference 24 show that the power performance and propagation delay of the proposed converter compared to the converter provided in the reference 24 are improved by 14.7 and 18.2 percent, respectively. It has been found that the number of transistors used in this converter is 59, which is 10.61 percent less than the presented converter.

The ternary to binary 3 to 5 converter has 3 inputs, which requires three decoder circuits. The simulation results of this proposed converter show that the average power consumption required for the conversion is equal to 0.87 microwatts. Also, the number of transistors required to implement this converter is 137. In Figure 26, outputs waveforms are shown for all possible states for inputs. In this figure, the vertical axis is the voltage level of the nodes. As can be seen in this figure, the performance of the converter is correct in all conditions, for example, for the input T="021", the output is B="00111".

In the Figure 29, The power consumption of TTBC 2×4 and TTBC 3×5 versus Temperature have been shown. According with Figure 29, the power of TTBCs are increased with temperature. And also, Figure 30 shows the waveform diagram of the TTBC(2×4) outputs for changes in the capacitance load.

Various works have been reported for the implementation of different types of ternary to binary converters using MOSFET and CNTFET technologies. The comparison table shows that the converters proposed in this article are relatively good in terms of space, power, and propagation delay. As reported in Table 14, the proposed TTBC5×8 has improved by 10% in terms of propagation delay, 6% in terms of power consumption, and 11% in terms of the number of transistors compared to the similar work reported, while the PDP index has improved by 15.5% compared to the reference. The figure of merit of converters is obtained by multiplying the number of transistors by PDP index.

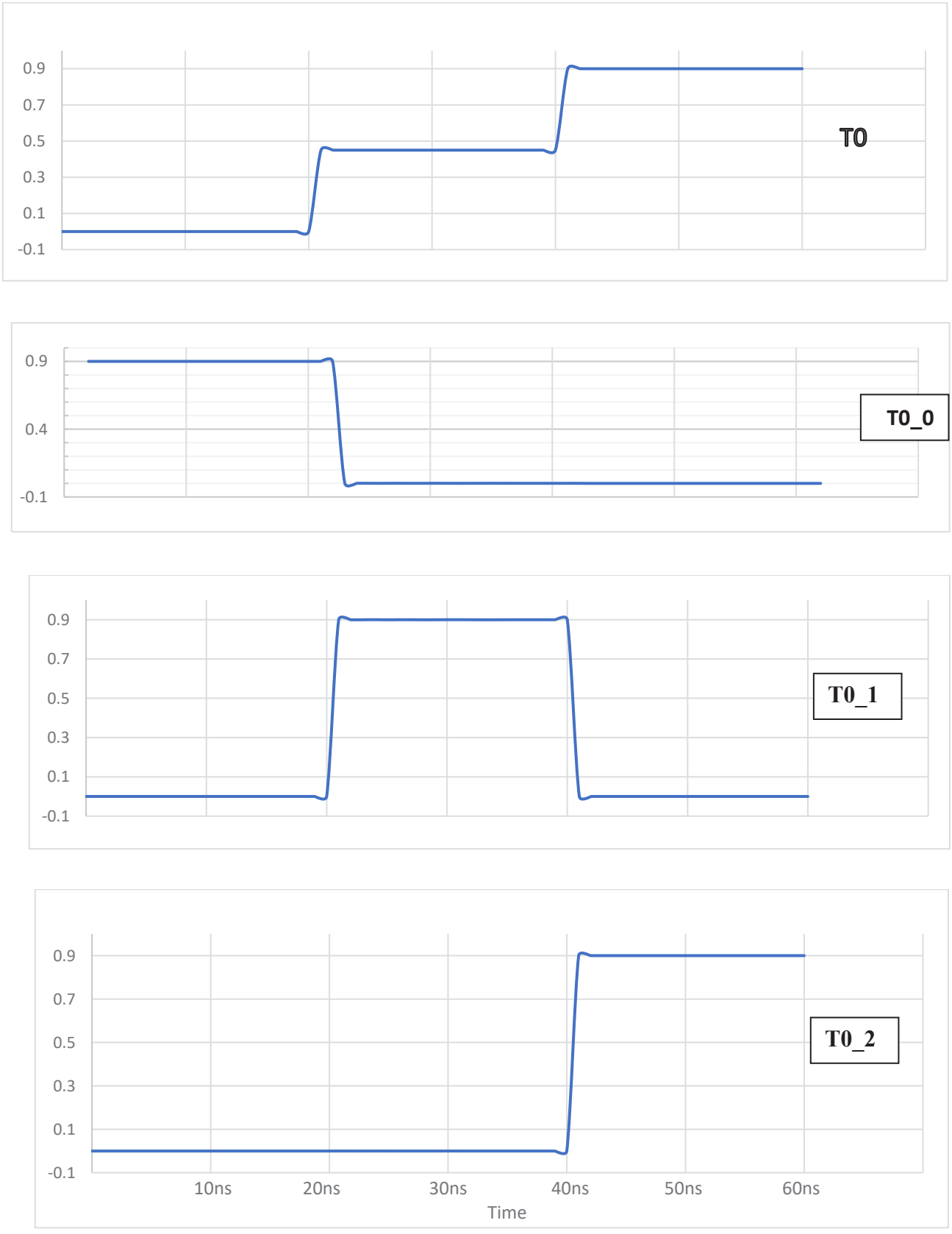

Fig. 26. Time diagram of decoder block outputs

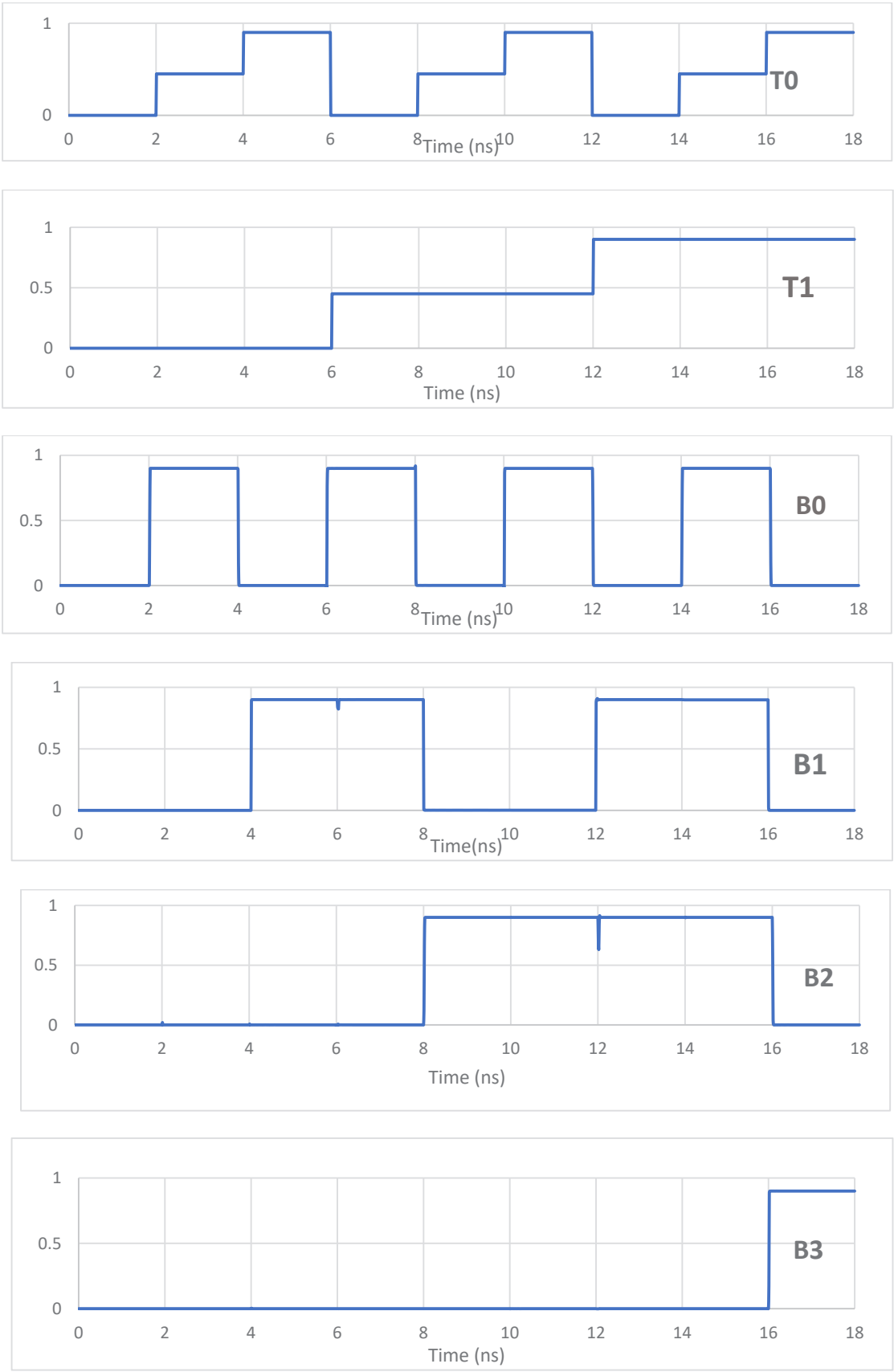

Fig.27. outputs waveforms of TTBC 2×4 converter

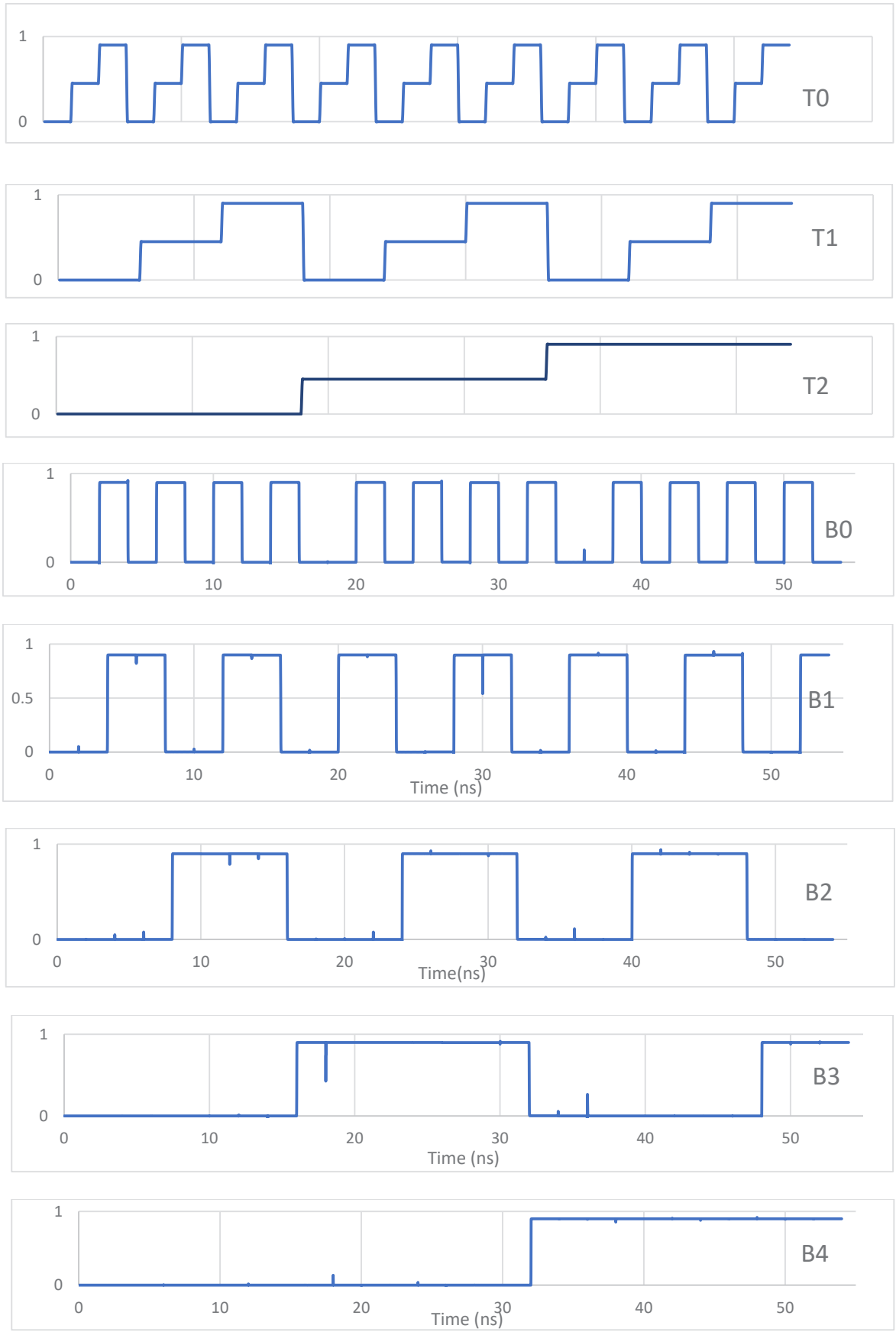

Fig. 28. outputs waveforms of TTBC 3×5 converter

Table 12. Simulation results of TTBC2×4 compared to the reference 24

Parameters	Proposed	24	Performance (%)
Power (µW)	0.295	0.346	**14.71**
Tpd (ps)	13.50	16.50	**18.18**
PDP(J)	3.98	5.71	**30.22**
EDP	53.77	94.16	**42.90**
N	57	66	**13.64**
FOM(N*EDP)	3.07	6.21	**49.43**

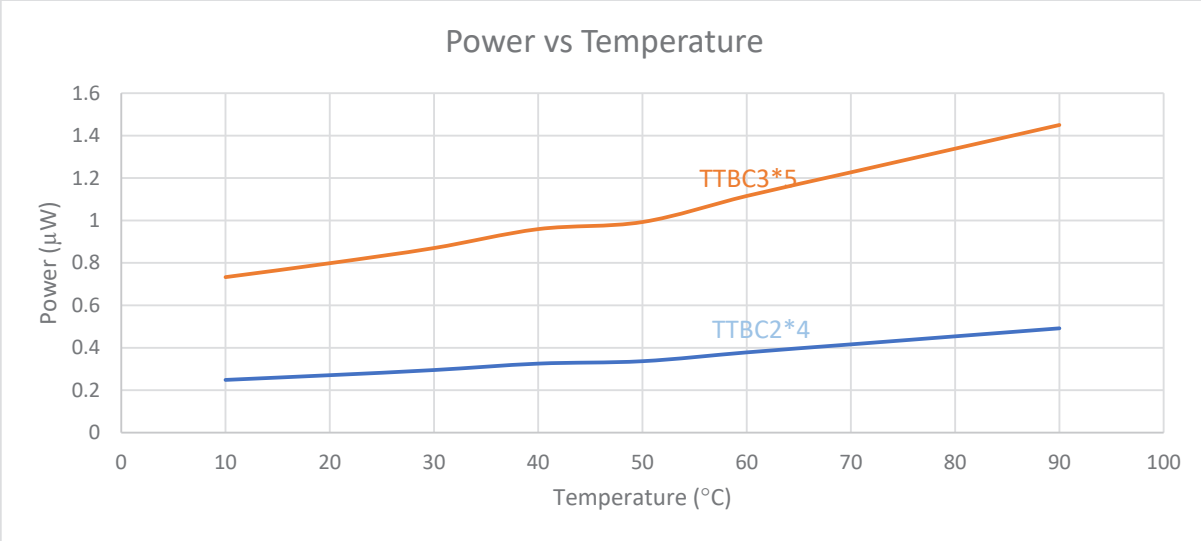

Fig. 29. Power consumption of TTBC (2:4) and TTBC (3:5) versus Temperature

Table 13. Simulation results of TTBC2×4 compared to the reference 24

Parameters	Proposed TTBC(3:5)	[24] TTBC(3:5)	Performance (%)
Power (uW)	0.87	1.143	**23.7**
T_{pd}(ps)	15.4	29	**46.9**
PDP (Power- Delay –Product)(10^{-18} J)	13.39	33.13	**59.6**
N	137	156	**13.87**
FOM @N*PDP(10^{-18})	1.83	5.17	**64.3**

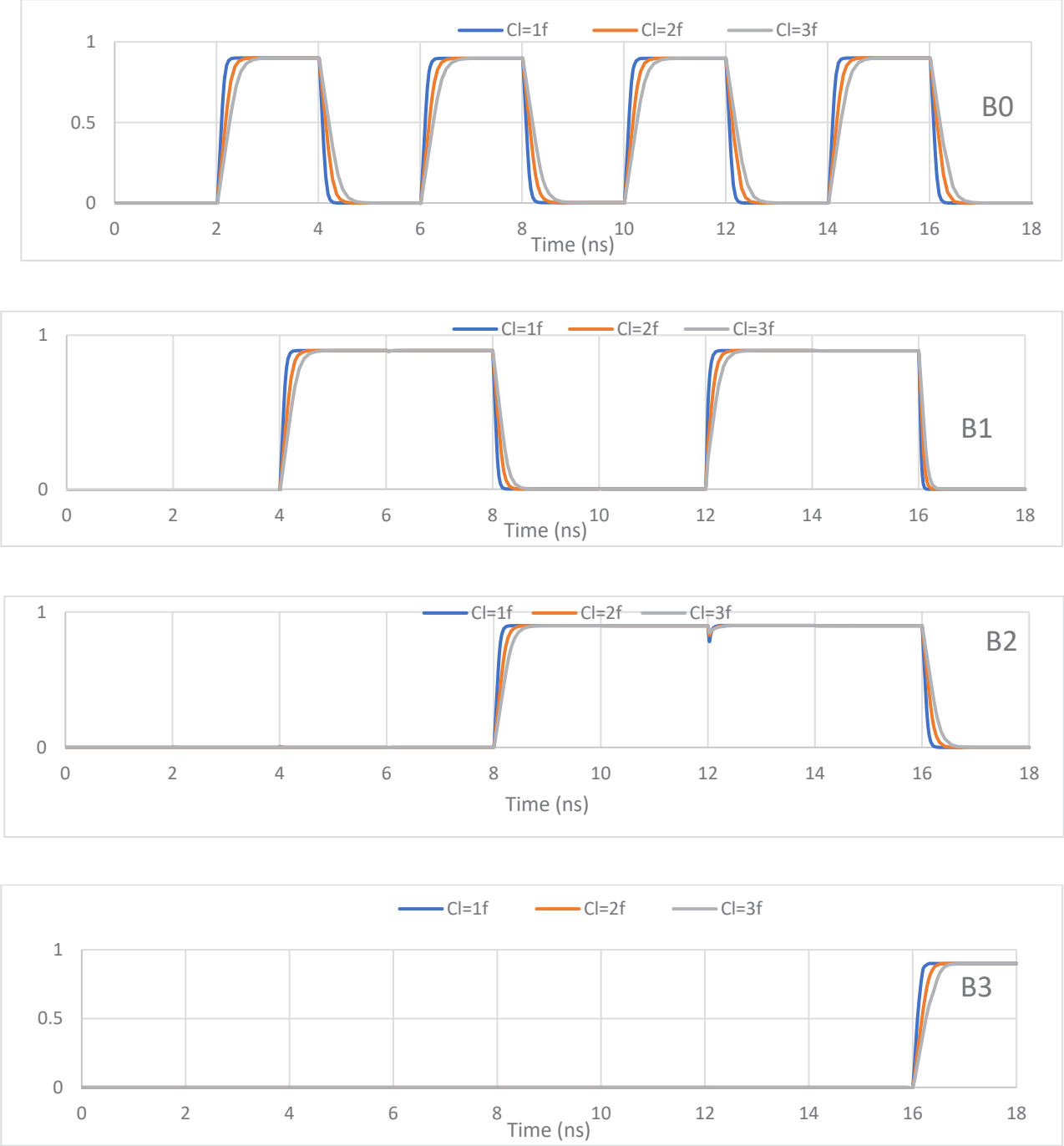

Fig. 30. Output waveforms of TTBC2*4 in the different CLOAD

Table 14. Comparing the parameters of proposed ternary to binary converters with other converters

References	TTBC	Number of Transistor	Technology (nm)	Power µW)	Propagation Delay ps	PDP aJ
[24]	4×7	270	CNTFET 32nm	1.59	54	**86.04**
[24]	5×8	410	CNTFET 32nm	2.01	58.1	**116.94**
Proposed	4×7	219	CNTFET 32nm	1.49	48	**71.52**
Proposed	5×8	365	CNTFET 32nm	1.89	52	**98.82**

5- Conclusion

According to the special features of CNTFE technology compared to other technologies, the circuits needed to implement multi-level systems are much simpler, and due to the increasing volume of signal processing and the increase of data and connections between blocks. It is necessary to move from the domain of binary design to the multi-level domain, therefore, to create a connection between binary and ternary signals, high-speed and low-power converters are needed, and in this article, how to implement a ternary-to-binary converters were reported. The results of this report show that the proposed converters have good performance compared to similar tasks. In this report, the circuits of ternary to binary single-input, two-input, three-input, four-input and five-input ternary converters were presented. And how to implement this The converters were explained using CNTFET transistors. HSPICE software is used to simulate the correct operation of the proposed circuits of these converters. The results show that the PDP index of the TTBC5×8 is equal to 98.82 aJ.

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