AUT Journal of Electrical Engineering

AUT J. Elec. Eng., 54(1) (2022) 49-66
DOI: 10.22060/eej.2021.20211.5423

Full Soft-Switching Ultra-High Gain DC/DC Converter Using Three-Winding Coupled-Inductor with Modular Scalability for Renewable Energy Applications

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ABSTRACT: This paper proposes a new non-isolated single-switch DC/DC converter with an ultra-high voltage gain, low input current ripple, low voltage stress, soft-switching operation, and modular scalability for renewable sources applications. With the help of a Three-Winding Coupled-Inductor (TWCI) and Voltage Multipliers circuits, ultra-high voltage gains can be achieved without needing a large duty cycle. A regenerative clamp capacitor recycles the energy stored in the leakage inductor; thus, the maximum voltage across the single power switch is restricted. Moreover, at the turn-on instant of the power switch, a Zero Current Switching (ZCS) condition is achieved. By designing a resonant tank, the switched current value of the main switch at the turn-off instant is reduced significantly. Additionally, the leakage inductor of the TWCI helps all converter diodes to operate under the ZCS condition. Due to full soft-switching performance, the introduced topology can provide a wide output voltage range under a high conversion efficiency. The steady-state analysis and comprehensive comparisons are provided in this paper. A 160 W prototype with 24 V input and 250 V output voltage is developed to validate the theoretical analysis. Due to ZCS operation and low voltage stress (VDS ≈ 40 V), the power loss portion of the MOSFET is low. Moreover, the maximum voltage stresses of diodes are measured as 40 V, 60 V, 90 V, and 110 V, that are well below the output voltage. Furthermore, at the full-load condition, the input current ripple is about 20 % and the measured efficiency is about 96.3%.

Review History:

Received: Jun. 30, 2021
Revised: Aug. 28, 2021
Accepted: Sep. 14, 2021
Available Online: Jun. 01, 2022

Keywords:

Step-Up DC-DC Converter
Ultra-High Gain
Three-Winding Coupled-Inductor (TWCI)
Soft-Switching
Voltage Multiplier (VM
Modular Scalability

1- Introduction

High step-up (high-gain) DC/DC converters play an important role in many applications, such as renewable energy sources (Photovoltaic and Fuel Cells), some medical devices, aircraft, automobiles, and street lighting. In such applications, step-up circuits act as interfacing circuits to convert the low input voltage to the desired high output voltage. However, in addition to high voltage gain, there are some critical requirements for appropriate performance, including low voltage stress, high efficiency, and low input current ripple [1, 2].

Theoretically, the conventional step-up topologies such as boost converter, can provide a high voltage gain ratio. However, due to increased power loss including switching power dissipations and output diode Reverse Recovery Problems (RRP), even high duty cycles cannot help in achieving a high voltage conversion ratio. The mentioned reasons force the experimental conversion gain of the boost converter to be limited (< 5) [3]. Due to these disadvantages, the designing of modified converters with more proper key performance indicators is necessary. For this purpose, some voltage boosting methods such as voltage lift [2], Switched-Capacitors (SC), Voltage Multiplier Rectifier/Cell (VMR/VMC) cells [4], Switched-Inductors (SI) [2], and cascading techniques have been presented [5].

In recent years, to improve the performance of the high voltage gain DC-DC converters, magnetic components such as Coupled-Inductors (CI) are also broadly employed [2]. In these circuits, with the help of the turn's ratio of the CI as an additional design factor, a higher voltage gain can be achieved. However, a voltage spike exists on the active switching devices in CI-based converters that can be restricted by the help of a clamp circuit [6]. It is noteworthy that hard-switching performance and diode reverse recovery issues often decrease the conversion efficiency of the many step-up converters. For this purpose, designing the resonant tank in the middle part of the circuits can be more profitable [7].

The main focus of many recent research studies has been presented as modified CI-based step-up, with soft-switching conditions. Using VMs and CI in the CI-based converters in [8], a high voltage conversion with a full soft-switching operation for all switching components is provided. However, Due to the series connection of CI series with the input source, these converters suffer from high input current ripple, limiting their applications for renewable energy sources. Additionally,

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new interleaved step-up converters are derived in [9, 10] by inserting two VMC. However, these multiple switch converters are suitable for high-current and high-power applications. In addition, new CI-based converters with very high voltage gain are provided in [11, 12]. However, due to the high input current ripple, they are not suitable for renewable sources. In references [13, 14], new types of single-switch high-voltage gain topologies with regenerative clamp circuits are presented. In these converters, the leakage inductor of the magnetic devices helps to create a resonant tank for soft-switching operation without any additional components, which leads to significant alleviation of the switching dissipations and RRP. Nevertheless, these converters cannot provide a wide range of voltage gain ratios. Furthurmore, several types of single-switch high gain DC-DC converters are introduced in [15]. Hard switching performance is a demerit of the mentioned converters. Another structure of step-up converter with resonant performance is suggested in [16]. However, due to the limited voltage gain ratio, this converter cannot be used in ultra-high voltage gain applications. An ultra-high voltage gain (semi-quadratic form) converter based on the cascading connection of boost and buck-boost converters is suggested in [17]. Despite achieving high voltage gains, using two active switches with hard-switching condition is the main downside of the mentioned converter. Moreover, a new type of Zero Voltage Transition (ZVT) step-up converter with low input current ripple is presented in [18]. The use of two switches is the main disadvantage of this circuit.

In references [19-21], with the help of a Three-Winding Coupled-Inductor (TWCI), a high voltage gain can be achieved by setting the secondary and tertiary turn ratios as an additional degree of design freedom. In these circuits, the leakage inductor of the CI helps to decrease the RRP of the diodes. Although the extreme duty cycle is avoided in the aforementioned converters, the input current ripple is large and detrimental to the lifetime of the renewable power sources. Moreover, in the case of TWCI [22], there is no common ground between the input and output load in addition to the large current ripple, which will lead to limited applications due to safety reasons. In [23], with the help of a TWCI, a soft-switching high gain converter is presented. Despite the suitable operating performance of the switches, the converter voltage gain has not been significantly extended. Furthermore, A dual active clamp DC-DC converter with high voltage gain is also suggested in [24]. Nevertheless, the voltage gain of the proposed three-switch isolated converter is limited. In [25, 26], ultra-high step-up DC-DC converters with low voltage stresses across semiconductor components are proposed. However, the most crucial disadvantage of these converters is the large input current ripple. In addition, in [27], a novel TWCI switch-mode converter with a high voltage conversion ratio is provided, although the voltage stress of the diodes in this converter is significant.

In this paper, to solve the earlier mentioned problems, a new type of full soft-switching DC/DC converter with an ultra-high gain based on a TWCI with high efficiency is presented. The outstanding merits of the proposed topology are ultra-high voltage gain ratio, low input current ripple, low voltage stress, full soft-switching operation for all switching components, and modular scalability. The VMR and VMC units, along with TWCI allow the suggested circuit to reach an ultra-high voltage gain with small duty cycles which leads to reduced power losses. In addition to the ZCS condition, implementing a QR operation decreases the switching loss as well as RRP loss, significantly.

This paper is organized as follows: the proposed circuit diagram and the steady-state analysis are presented in Sections II and III. Section IV describes the comparison of the proposed topology and other related converters. Design considerations of the converter components are presented in Section V. The experimental results of the voltage and current of the components for a sample prototype are presented in section VI. Finally, the conclusions are provided in Section VII.

2- Circuit Description of the Proposed Converter

The structure of the proposed circuit is shown in Fig. 1. This topology is comprised of a single power switch, a TWCI with two outputs (secondary and tertiary), an input inductor (L_{in}), a VMR unit (D_1, D_2, C_1, C_2, and N_2), and a VMC unit (D_3, D_4, C_4, C_5, and N_3). The turn's ratio of the primary, secondary, and tertiary sides of the TWCI are listed as N_1: N_2: N_3, respectively. A flowchart of step-by-step structure design procedure of the proposed converter is also shown in Fig.2. Using two types of VM, including VMC and VMR, made the presented circuit able to increase the voltage conversion ratio by setting the turn ratios of the TWCI. To further increase the output voltage while reducing the voltage stresses across the component in this topology, more VMs can be modularized. Moreover, the voltage stress on the single power switch is limited by a regenerative clamp circuit D_c and C_c. In the presented converter, due to considering a resonant tank among the leakage inductance of the TWCI and the middle capacitors, the current shapes of the power switch and the diodes D_1, D_2, D_4, and D_o change as a sinusoidal form, which alleviates the switch turn-off loss and removes the RRP, significantly. To simplify the proposed circuit analysis, the following assumptions are made:

The switching devices (switch and diodes) are considered ideal.

All capacitors of the converter are large enough, hence their voltages are to be constant.

The magnetic device (TWCI) is modeled as an ideal transformer with a magnetizing inductor (L_M), and a merged leakage inductor (L_k) with the turn's ratios of $n_{21}=N_2/N_1$ and $n_{31}=N_3/N_1$ for secondary and tertiary sides, respectively.

Fig. 3 shows the key waveforms of the main components of the converter, which include six operational modes. Moreover, the equivalent circuits of the operating modes are depicted in Fig. 4.

Mode 1 [t_0-t_1]: At $t=t_0$, the single power switch S starts to conduct at ZCS condition. Diode D_3 is conducting in Fig. 4 (a), and other diodes of the circuit are in reverse bias. During this mode, the input and magnetizing inductors (L_{in} and L_m) begin

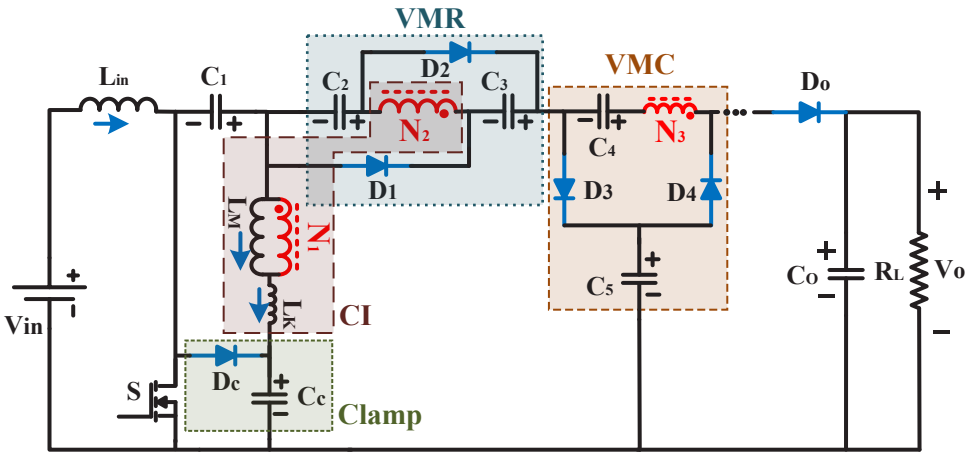


Fig. 1. Structure of the proposed ultra voltage gain DC-DC converter.

to receive energy from the input DC source and the capacitor C_1, respectively; hence their currents increase linearly. Due to the presents of leakage inductor on the secondary side of the TWCI, diode D_3 turns off with a slow slip, with Low Reverse Recovery (LRR) loss at the end of this mode.

Mode 2 [t_1-t_2]: In this mode, the single power switch remains on. The diodes D_1, D_2, and D_4 start to conduct at ZCS conditions. The inductors L_{in} and L_m will charge same as Mode 1. In addition, the energy saved in C_5 is transferred to C_4. In this time duration, a tank resonant including the leakage inductor L_k and the middle capacitors is created, which discharges the energy of the clamp capacitor C_c. Regarding Fig. 3, this QR performance leads to sinusoidal changes in the main power switch current, diodes D_1, D_2, and D_4. Consequently, the current value of the switch is alleviated at the end of this mode, which decreases the turn-off dissipation. Eq. (1) shows the resonant frequency during operating mode 2 (f_{R2}).

$$f_{R2}=\frac{1}{T_{R2}}=\frac{1}{2\pi}\sqrt{\frac{\left(\frac{1}{C_1}+\frac{1}{C_c}\right)\frac{\gamma}{\beta}-\frac{1}{C_1}}{L_k\frac{\gamma}{\beta}}} \quad (1)$$

Here, the parameters γ and β are defined as follows:

$$\gamma=\frac{1-n_{31}}{2C_3}+\frac{1}{C_1}+\frac{1}{C_4}+\frac{1}{C_5} \quad (2)$$

$$\beta=\frac{1}{2C_3}+\frac{n_{21}}{C_1} \quad (3)$$

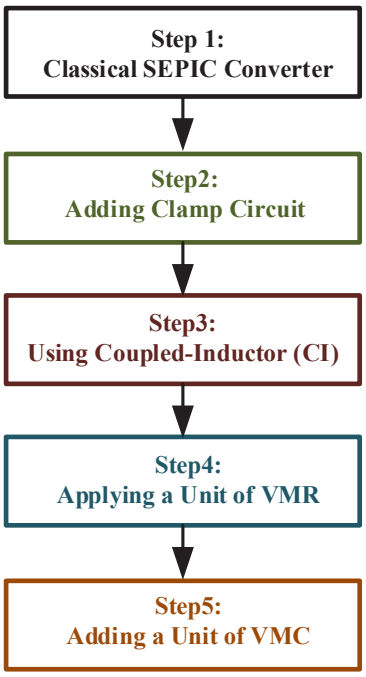


Fig. 2. Flowchart of the step-by-step structure design procedure of the proposed converter.

According to key waveforms in Fig. 3, to achieve the minimum turn-off loss for the switch, half of the resonant time ($0.5T_R$) should be less or equal to the pulse width ($\frac{T_R}{2}\le DT_s$). During this time operation, the equations (4)-(8) are also given:

$$v_{Lin}=V_{in} \quad (4)$$

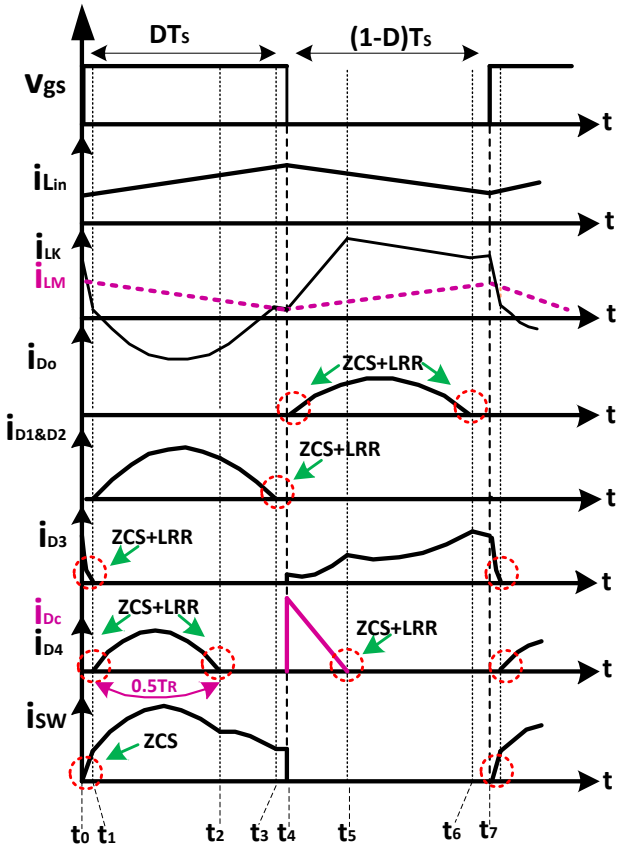


Fig. 3. Key waveforms of the presented converter components (LRR =Low Reverse Recovery).

$$v_{LM} = v_{C1} - v_{Cc} \tag{5}$$

$$v_{C2} = v_{C3} = n_{21} v_{LM} \tag{6}$$

$$v_{C4} = v_{C5} - v_{C1} - v_{C2} - n_{31} v_{LM} \tag{7}$$

$$i_{SW} = i_{in} - i_{LK} + i_{D4} \tag{8}$$

This mode is ended when the current of D_4 reaches zero naturally with LRR.

Mode 3 [t_2-t_3]: During operating mode 3, the capacitors C_2 and C_3 start to charge from the magnetizing inductor L_m of the TWCI. This mode is finished when the current of the diodes D_1 and D_2 reach zero at the ZCS conditions with LRR.

Mode 4 [t_3-t_4]: In this transient duration, the power switch S remains on-state, while all diodes of the converter are in reverse bias. Regarding Fig. 4 (d), the currents passed through the leakage, and magnetizing inductors (L_k and L_m) are identical. During this mode, the capacitor C_1 received energy from C_c. The passed through current value from the power switch (Eq. (9)) is expressed as:

$$i_{Sw} = i_{in} - i_{LM} \tag{9}$$

Mode 5 [t_4-t_5]: After switch S is turned off, the voltage stress is restricted by conducting the clamp diode D_c. Moreover, the current of D_3 and D_o begin to conduct at ZCS. Moreover, C_o and C_5 start to charge by the energy stored in L_{in}, L_m, C_1, and C_2. Thus, the input and magnetizing inductor's current (i_{Lin} and i_{LM}) decrease linearly. The current of the clamp diode D_c reaches zero naturally under the LRR problem at the end of this mode. The equations (10)-(13) can be derived in this mode:

$$v_{Lin} = V_{in} - V_{Cc} \tag{10}$$

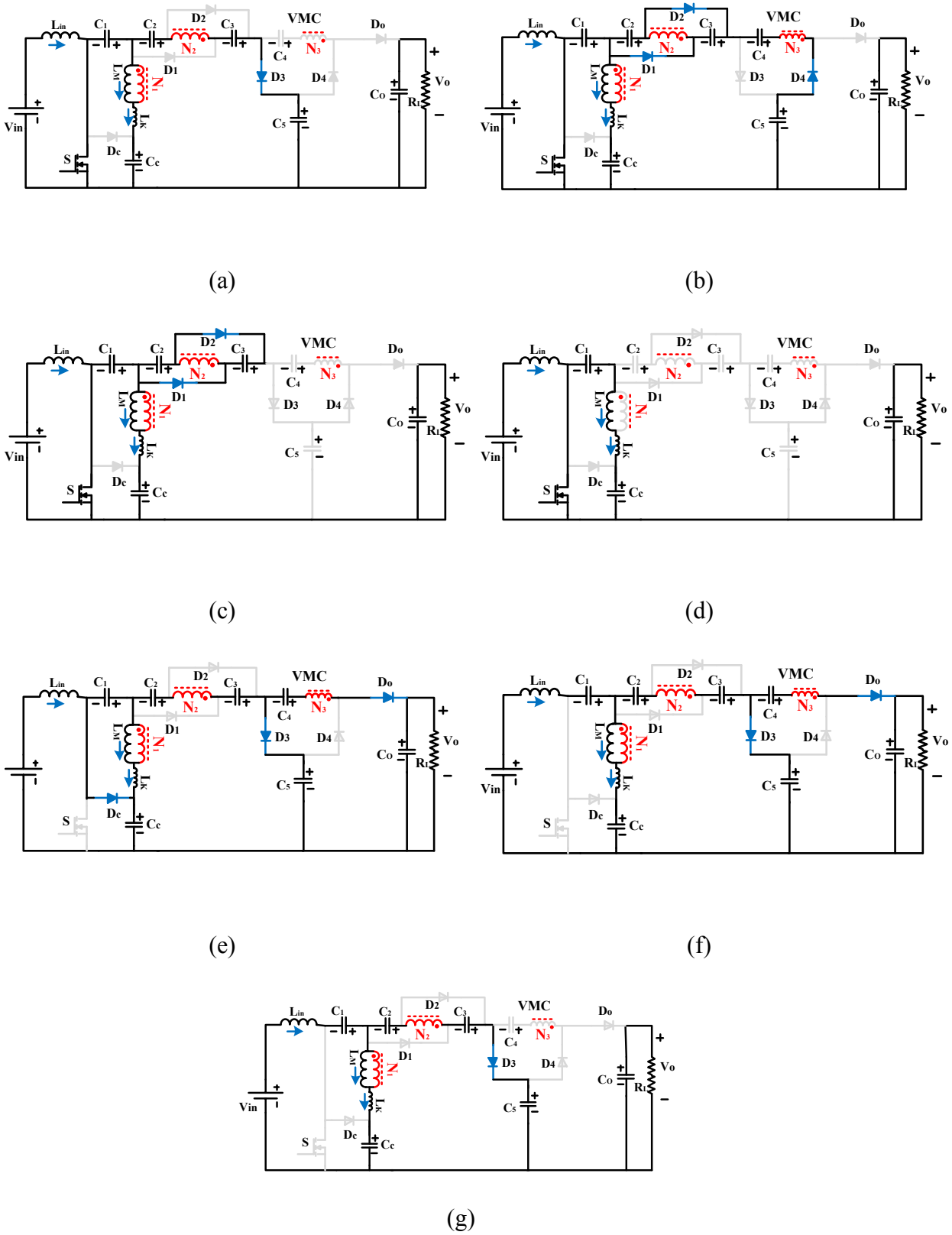


Fig. 4. The operation modes of the proposed converter, (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (f), Mode 7.

$$v_{LM} = V_{Cc} \tag{11}$$

$$V_{C5} = V_{Cc} + V_{C1} + V_{C2} + V_{C3} + n_{21} v_{LM} \tag{12}$$

$$V_o = V_{C5} + V_{C4} + n_{31} v_{LM} \tag{13}$$

Mode 6 [t_5-t_6]: In this interval, the diodes D_3 and D_o remain on-state. The output capacitor C_o and C_5 charge similar to mode 5. A QR between the leakage inductor of CI (L_k) and middle capacitors of the proposed converter is created, which leads to a sinusoidal form in the current of D_o.

Mode 7 [t_5-t_6]: At t_5, the output diode D_o turns off at a very low slope without reverse recovery problem. Additionally, the C_5 capacitor of the VMC unit starts to charge from the magnetic devices and capacitors C_2 and C_3.

3- Steady-State Performance Analysis

3- 1- Voltage Gain

The average value of the voltage of capacitors C_c (Eq. (14)) and C_1 (Eq. (15)) can be obtained by applying volt-second balance on L_{in} and L_m as:

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{14}$$

$$V_{C1} = \frac{DV_{in}}{1-D} \tag{15}$$

Where D denotes the duty cycle of the main power switch. Using Eq. (13), Eq. (14), Eq. (5), and Eq. (6), the voltage across capacitors C_2 and C_3 is founded in Eq. (16) as:

$$V_{C2} = V_{C3} = n_{21} V_{in} \tag{16}$$

By substituting Eq. (14)-(16) into Eq. (12), the average voltage of capacitor C_5 is calculated as:

$$V_{C5} = \frac{1 + D + n_{21}(2-D)}{1-D} \tag{17}$$

Regarding Mode II, the voltage of capacitor C_4 (Eq. (18)) is derived using Eq. (7), Eq. (15), and Eq. (16) as:

$$V_{C4} = \frac{1 + n_{21} + n_{31}(1-D)}{1-D} \tag{18}$$

Finally, by substituting the equations Eq. (14), Eq. (17)-(18) into Eq. (13), the voltage conversion ratio of the proposed circuit (Eq. (19)) in CCM operation is obtained as:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{2 + D + n_{21}(3-D) + n_{31}}{1-D} \tag{19}$$

According to equation Eq. (19), a wide range of voltage gain can be obtained by adjusting three degrees of freedom, including n_{21}, and n_{31}, and D. The voltage gain ratio of the presented topology as a function of duty cycle under different values of secondary and tertiary turns (n_{21} and n_{31}), are depicted in Fig. 5. Additionally, Fig. 6 plotted a 3D plot of the suggested converter voltage gain as a function of n_{31} and n_{21} for different duty cycles D=0.45, D=0.55, and D=0.65. Demonsttating these figures, an ultra-high voltage conversion ratio can be achieved at low duty cycles. Due to the more noticeable effect of the secondary winding turn ratio on the voltage conversion ratio, using a larger value of n_{21} rather than n_{31} leads to less wire consumption of CI.

3- 2- Voltage and Current Stresses

Using Eq. (14) and Eq. (19), the drain to source voltage across the main power switch and the voltage stress across clamp diode D_c (Eq. (20)) are given as:

$$V_{DS} = V_{Dc} = \frac{V_{in}}{1-D} = \frac{V_o}{2 + D + n_{21}(3-D) + n_{31}} \tag{20}$$

Moreover, Eq. (21)-(23) calculate the maximum voltage across the diodes D_1, D_2, D_3, D_4, and D_o as follows:

$$V_{D1} = V_{D2} = \frac{1 + n_{21}(1 + n_{21}(1-D))}{(1+n_{21})(2 + D + n_{21}(3-D) + n_{31})} V_o \tag{21}$$

$$V_{D3} = \frac{1 + n_{21}}{2 + D + n_{21}(3-D) + n_{31}} V_o \tag{22}$$

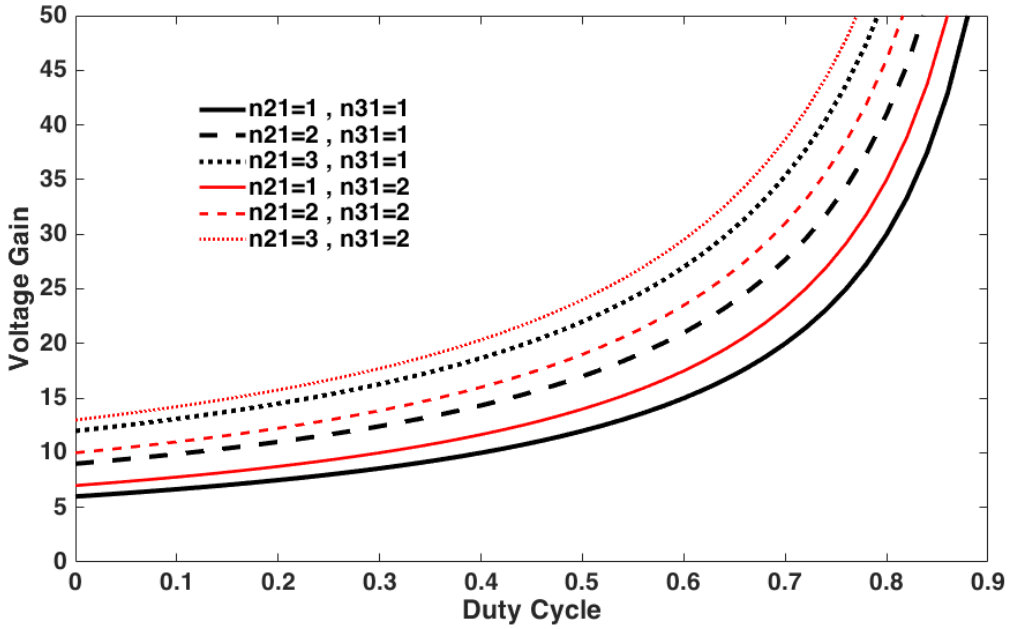


Fig. 5. The voltage gain of the proposed converter is a function of the duty cycle for several n21 and n31.

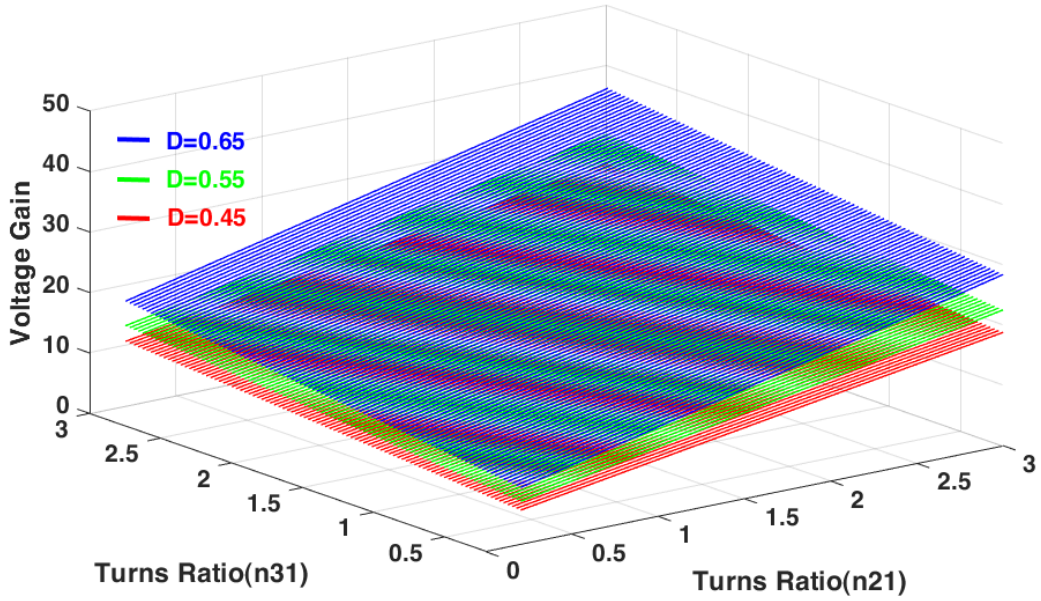


Fig. 6. 3D plot of the proposed converter voltage gain as a function of n31 and n21 for the different duty cycles D=0.45, D=0.55, and D=0.65.

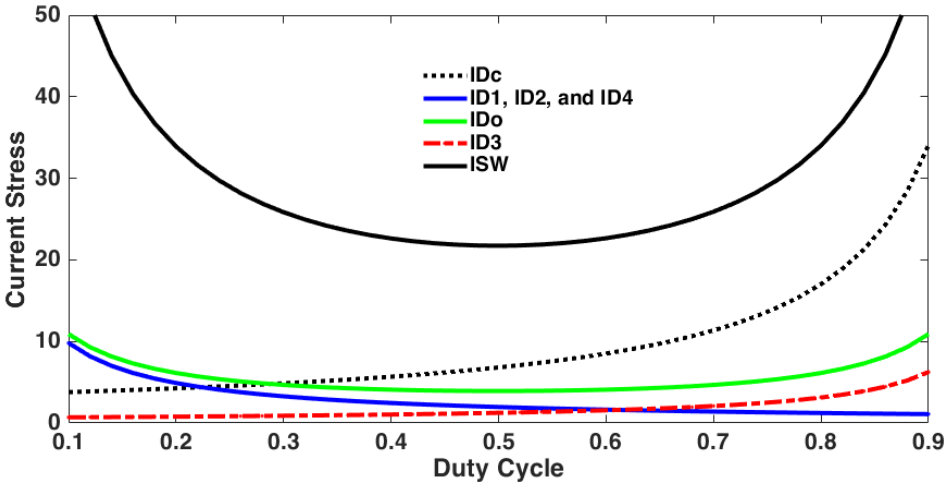


Fig. 7. Maximum current stress across the single power switch and the diodes of the proposed circuit at n21=1 and n31=0.5.

$$V_{Do} = V_{D4} = \frac{1 + n_{21} + n_{31}}{2 + D + n_{21}(3 - D) + n_{31}} V_o \quad (23)$$

Furthurmore, by applying the ampere-second law for the converter capacitors, the average current passed through of the magnetizing inductor L_m (Eq. (24)) is achieved by the equasion below, where I_o is the load current

$$< i_{LM} >= (n_{21} - 1) I_O \quad (24)$$

Considering the critical mode operation of the QR performance ($0.5T_R \approx D.T_S$), the peak current of diodes D_1, D_2, and D_4 is estimated in Eq. (25) as:

$$i_{D1\_peak} = i_{D2\_peak} = i_{D4_{peak}} = \frac{\pi}{2D} I_o \quad (25)$$

Furthermore, the peak value of the current of D_o and D_3 (Eq. (26) and (27)) are found by:

$$i_{Do\_peak} \approx \frac{\pi T_s}{T_R.(1-D)} I_o = \frac{\pi}{2D.(1-D)} I_o \quad (26)$$

$$i_{D3\_peak} = \frac{I_o}{1-D} \quad (27)$$

From (8) and (25), Eq. (26)-(27) show the real and maximum values of the switch current as:

$$i_S(t) \approx (M - n_{21} + 1) I_o + \quad (28)$$

$$(2n_{21} + n_{31} + 1) \frac{\pi}{2D} I_o \sin(w_{R2} t)$$

$$i_{S\_peak} = \left[M - n_{21} + 1 + (2n_{21} + n_{31} + 1) \frac{\pi}{2D} I_o \right] \quad (29)$$

Here, M represents the voltage gain of the proposed topology. According to operating mode 4 in Fig.4 (d), the current value of the power switch at the turn-off time, along with the stress current value passing through clamp diode D_c, is achieved is Eq. (30) as:

$$i_{SW}^{t=off} = i_{Dc\_peak} = (M - n_{21} + 1) I_o \quad (30)$$

Fig. 7 illustrates the maximum current stress of switching devices as a function of duty cycle under turns ratios n_{21}=1 and n_{31}=0.5. Illustrating from this figure, the minimum current stress for a single power switch has occurred at the duty cycle range 0.4<D<0.7.

4- Performance Comparison

To justify the advantages of the presented converter, an analytical comparison is provided with its other non-isolated

Table 1. Comparison between the proposed topology with other related converters.

Ref.	Components S/D/C/CI+L	Voltage Gain ratio	LICR	Voltage Stress on Power Switch	Voltage Stress on Output Diodes	SS	RRL	Eff. 100 W
[11]	2/6/6/1^{2W}+0	$\frac{(2+D)n}{(1-D)}$	No	$\frac{V_o}{(2+D)n}$	$\frac{(n-1)V_o}{(2+D)n}$	ZVS	Very Low	96.8%
[12]	2/6/6/1^{2W} +1	$\frac{1+2n(1-D)}{(1-D)^2}$	No	$\frac{V_o}{1+2n(1-D)}$	$\frac{2n(1-D)V_o}{1+2n(1-D)}$	ZVS+ ZCS	Very Low	97%
[13]	1/4/5/1^{2w} +1	$\frac{1+D+n(2-D)}{(1-D)}$	Yes	$\frac{V_o}{1+D+n(2-D)}$	$\frac{(1+n)V_o}{1+D+n(2-D)}$	ZCS+ QR	Very Low	97.0%
[14]	1/4/5/1^{2w} +1	$\frac{1+n(1+D)}{(1-D)}$	Yes	$\frac{V_o}{1+n(1+D)}$	$\frac{(1+n)V_o}{1+n(1+D)}$	ZCS+ QR	Very Low	96.8%
[15]	1/5/6/1^{2w} +1	$\frac{2(1+n)}{(1-D)}$	Yes	$\frac{V_o}{2(1+n)}$	$3\times\frac{1+2n(1-D)V_o}{2(1+n)}$	ZCS	Low	96.4%
[16]	1/3/4/1^{2w} +1	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZCS+ QR	Very Low	96.8%
[18]	2/6/7/1^{3W} +1	$\frac{2(n_2+n_3)+3}{(1-D)}$	Yes	$\frac{V_o}{2(n_2+n_3)+3}$	$\frac{(1+n_2+n_3)V_o}{2(n_2+n_3)+3}$	ZVT	Low	96.1%
[21]	1/8/8/1^{2w} +0	$\frac{4+n(2-D)-D}{(1-D)}$	No	$\frac{V_o}{4+n(2-D)-D}$	$\frac{(n(2-D)-D)V_o}{4+n(2-D)-D}$	-	Medium	93.6%
[23]	1/5/6/1^{3W} +1	$\frac{n_2+n_3+1}{(1-D)}$	Yes	$\frac{V_o}{n_2+n_3+1}$	$\frac{(n_2+n_3)V_o}{n_2+n_3+1}$	ZVS+ ZCS	Very Low	96.2%
This Work	1/6/7/1^{3W} +1	$\frac{2+D+n_2(3-D)+n_3}{(1-D)}$	Yes	$\frac{V_o}{2+D+n_2(3-D)-n_3}$	$\frac{(n_2+n_3+1)V_o}{2+D+n_2(3-D)-n_3}$	ZCS+ QR	Very Low	96.8%

S=Switch, **D**=Diode, **C**=Capacitor, **CI** =Coupled-Inductor, **L**=Inductor, **LICR**= Low Input Current Ripple, **SS**=soft-switching **Eff**=Efficiency, **RRL**= Reverse Recovery Loss.

counterparts proposed in recent years, which is summarized in Table 1.

Fig. 8 (a) and (b) depict the voltage gain comparison along with the voltage gain per number of the components between the converter and other counterparts referred to in Table 1 at the same conditions of turns ratio (n_{21}=1.5 and n_{31}=0.5 for TWCI-based converters) ($n=n_{21}+n_{31}$=2 for CI-based converters).

Illustrating from Fig. 8 (a), the suggested circuit in this paper can provide a higher voltage gain ratio, along with the converters in [18] and [21]. Nevertheless, using more semiconductor components and large input current ripple are the main disadvantages of the converters [18] and [21], which limit these converters' applications. Additionally, illustrating from Fig. 8 (b), the voltage gain ratio to the number of elements used in the proposed converter is at a high level. Fig. 9 (a) and (b) show the normalized voltage stress across single power switch and output diode, respectively. As can be demonstrated, the lower voltage stress on the switch of the presented topology makes it possible to choose a switch with lower parasitic components ($R_{DS(on)}$), which alleviates its power loss. In addition, the QR performance for the main power switch and all diodes of the proposed converter decrease the switching dissipations and improves efficiency. Moreover, a comparison of efficiency has been performed for the converters in Table 1 under the same conditions (V_{in}=24 V, V_{out}=250 V, P_{out}=100 W, f_s=60 kHz). The parasitic components are also extracted through related catalogs. According to these analyzes, the proposed converter has an acceptable efficiency than other converters.

5- Design Procedure of the Key Components

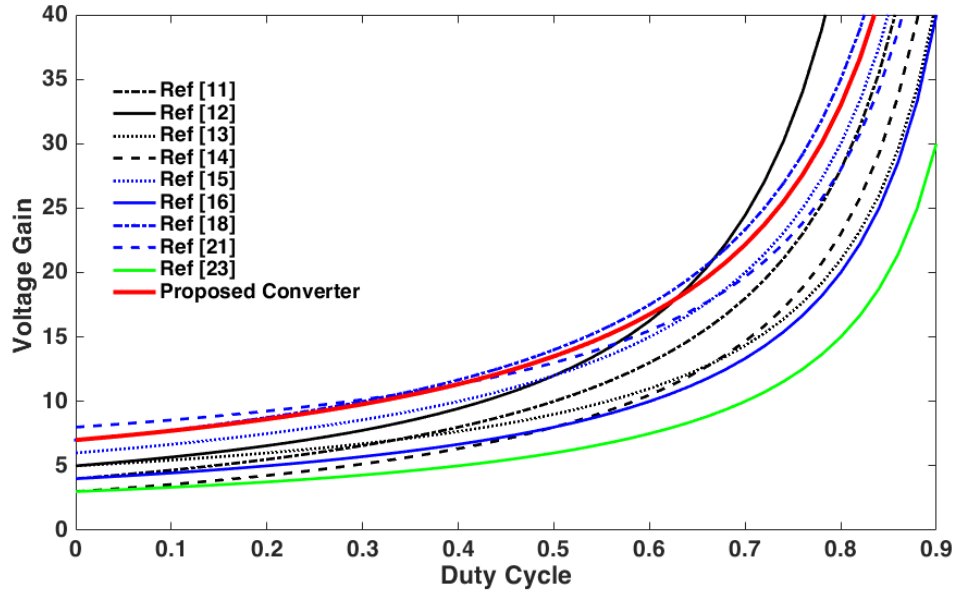
5- 1- Input and Magnetizing Inductors

The minimum value of the input inductor (Eq. (31)) is calculated to guarantee the CCM operation (to prolong the usage life of renewable sources) as:

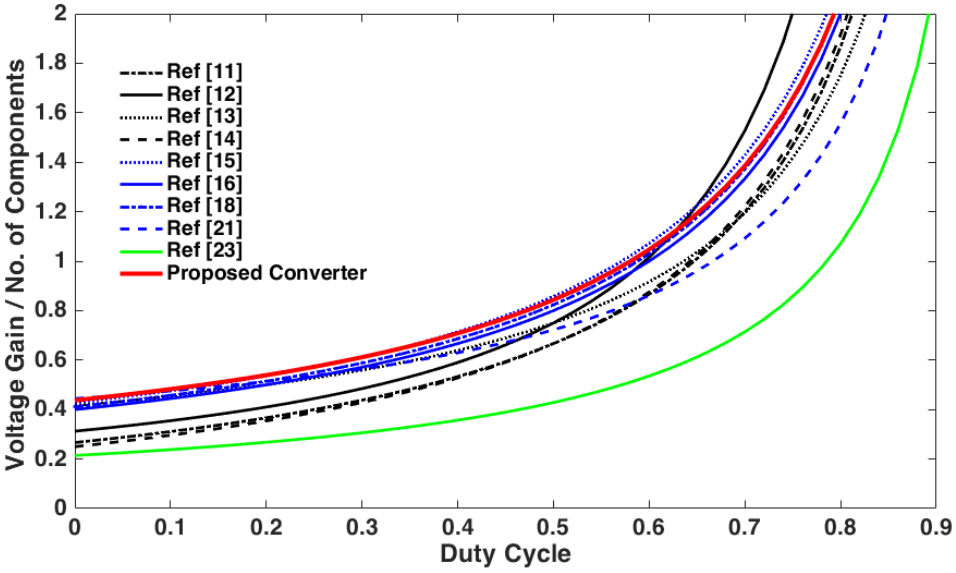
$$L_{in} > \frac{V_{in}.D}{\Delta I_{in} f_s} \tag{31}$$

Here, ΔI_{in} is the allowable current ripple. Additionally, Eq. (32) gives the magnetizing inductor of the TWCI as:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM} f_s} \tag{32}$$

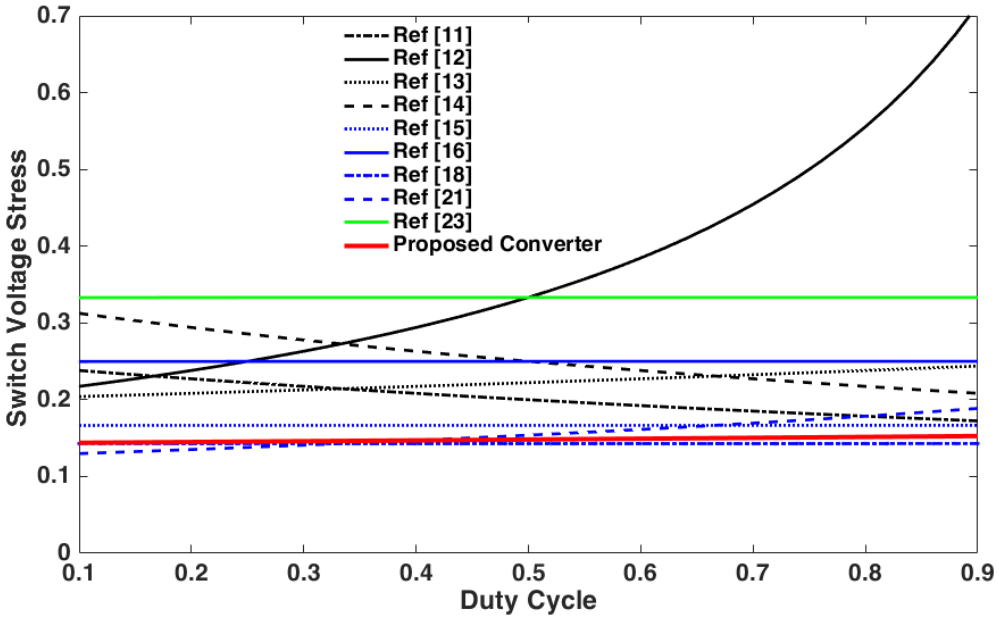


(a)

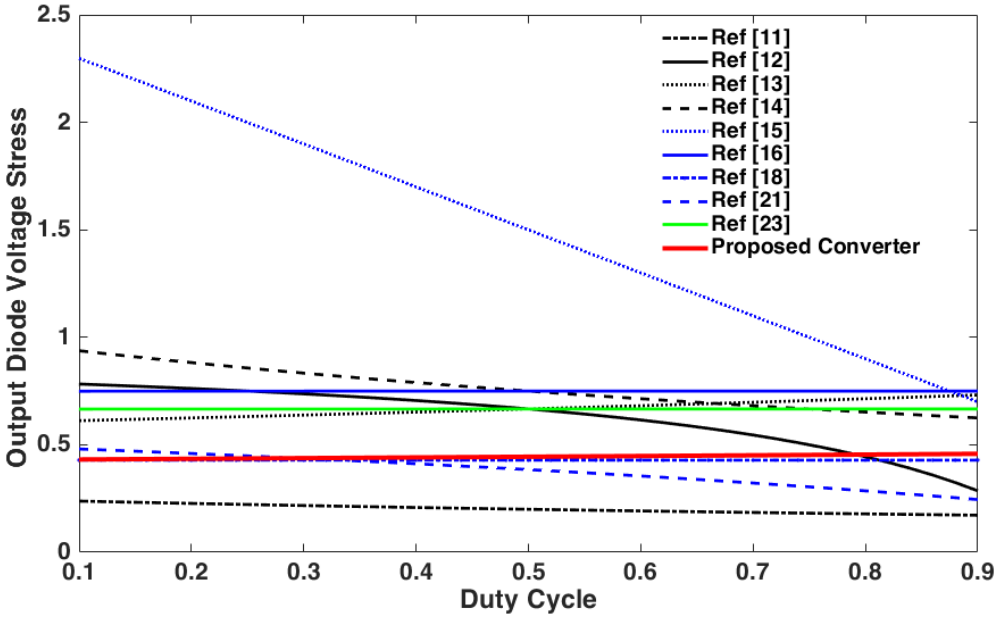


(b)

Fig. 8. (a) The voltage gain comparison, (b) The voltage gain per number of components comparison.



(a)



(b)

Fig. 9. (a) Normalized voltage stress comparison, (b) normalized voltage stress comparison.

Table 2. Parameters and components used in the laboratory prototype.

Parameter	Values
Output Power	160 W
Input DC Voltage	24 V
Output DC Voltage	250 V
Switching Frequency	55 kHz
Capacitors C_2, C_3 and C_5	47 µF / 250 V
Capacitor C_4	4.7 µF / 250 V
Capacitor C_1	47 µF / 160 V
Capacitor C_c	3.3 µF / 100 V
Capacitor C_o	100 µF / 250 V
Power Switch	IRFP4310 / $R_{DS(on)}$=5.6 mΩ
Input Inductor L_{in}	160 µH / T184-52
Magnetizing Inductor	180 µH
Turn Ratios of the TWCI (N_1:N_2:N_3)	(24:24:12) / EE42/21/20
Merged Leakage Inductance L_K	4.4 µH
Diodes D_c, D_1 and D_2	SR360 (VF (Max)=0.7 V)
Diodes D_4 and D_3	MUR420 (VF (Max)=0.88 V)

Where ΔI_{LM} is the current ripple.

5.2 Capacitors Selection

In order to achieve the output DC voltage in a constant value, the output capacitor C_o can be expressed by Eq. (33):

$$C_o = \frac{DV_{out}}{R_L.\Delta V_{co}.f_s} \tag{33}$$

Here, ΔV_{Co} denotes the maximum tolerant voltage ripple. Eq. (34)-(37) show the proper selection of the middle capacitors of the converter as:

$$C_1 = \frac{i_{Lin}.(1-\mathrm{D})}{\Delta V_{c1}.f_s} \tag{34}$$

$$C_2 = C_3 = \frac{(i_{D3}+i_{Do})(1-\mathrm{D})}{\Delta V_{c2}.f_s} \tag{35}$$

$$C_4 = C_5 = \frac{i_{D3}(\mathrm{D})}{\Delta V_{c3}.f_s} \tag{36}$$

$$C_c = \frac{(i_{LM}+i_{Dc})(1-\mathrm{D})}{\Delta V_{Cc}.f_s} \tag{37}$$

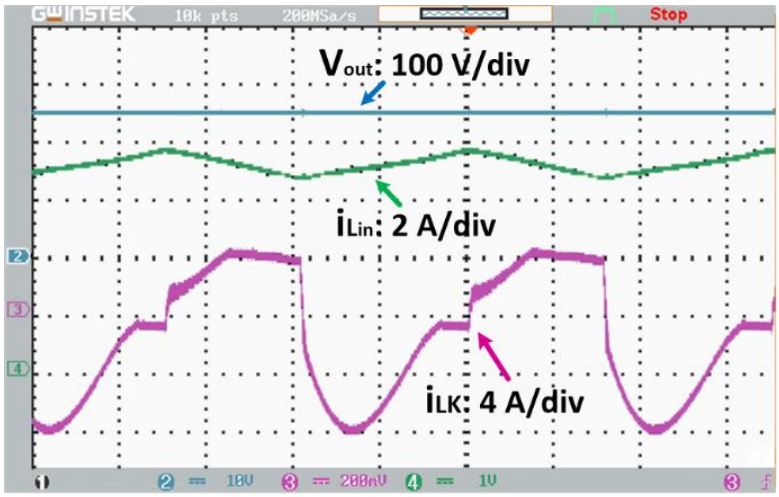
According to operation mode 2 and equation (1), the QR frequency is a function of the capacitors C_1 and C_c. Thus, these capacitors are also calculated by Eq. (38) as:

$$\pi\sqrt{\frac{L_k\frac{\gamma}{\beta}}{\left(\frac{1}{C_1}+\frac{1}{C_c}\right)\frac{\gamma}{\beta}-\frac{1}{C_1}}} = DT_S \tag{38}$$

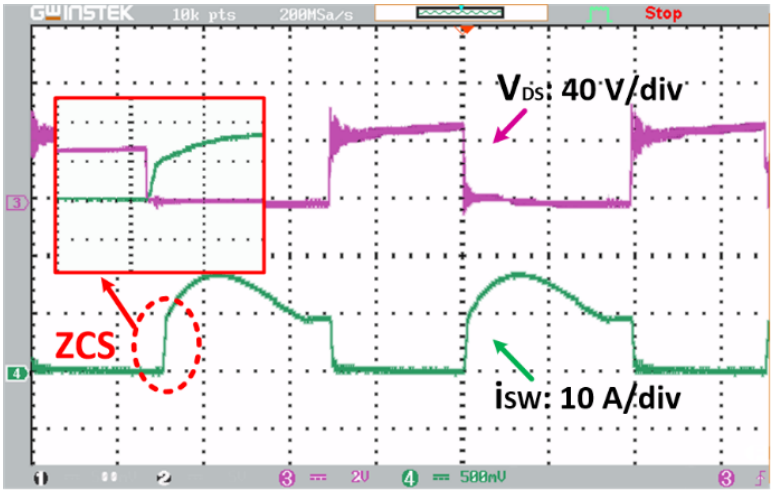
6- Experimental Verification

In order to justify the theoretical analysis of the proposed converter, a 160 W / 24 V-250 V sample prototype is implemented. The specifications of the prototype parameters are listed in Table 2. Due to the low voltage spike on the switch, a MOSFET with a low $R_{DS(on)}$ can be selected. The current and voltage waveforms of the circuit components were achieved using a high-frequency current probe PA-667 1 MHz and a differential voltage probe GDP-025. The experimental results are shown in Fig. 10 – Fig. 14.

The currents passed through the input and the leakage inductors, and the output DC voltage are illustrated in Fig. 10



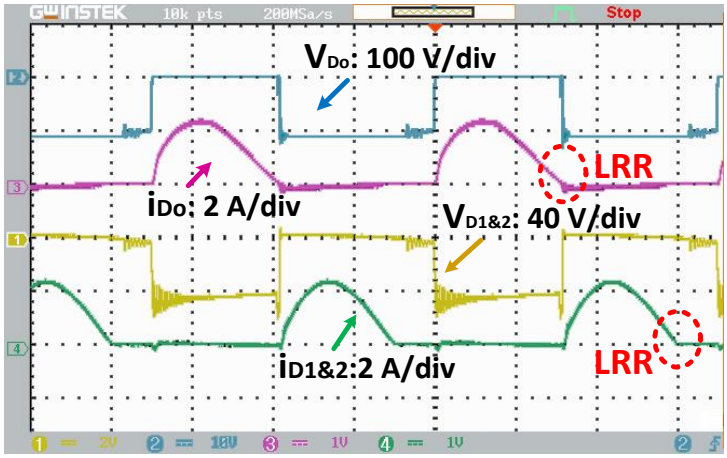
(a)



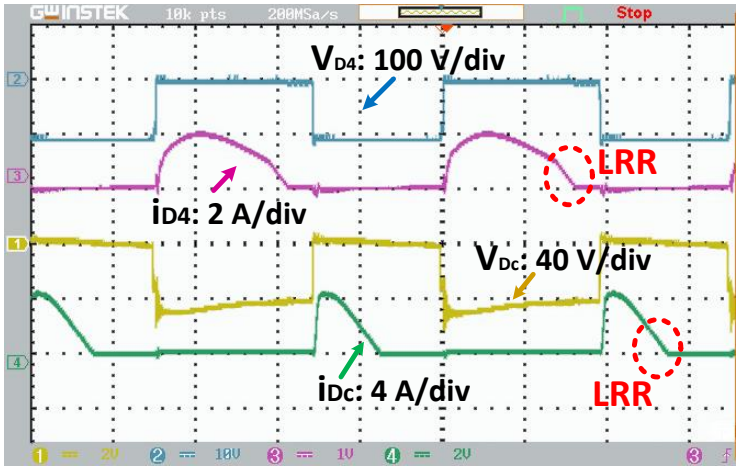
(b)

Fig. 10. Experimental results of the presented converter under the full-load of 160 W, (a) output voltage along with the current of the input and the leakage inductors, (b) voltage and current of the power MOSFET.

(a). As shown in this figure, the input current is the continuous form with a low ripple. According to Fig. 10 (b), the power MOSFET turns on under ZCS condition with a low voltage spike, which is clearly shown in this figure. Due to the QR operation, the current value of the switch at turn-off instant is alleviated, which reduces the turned-off power dissipation. Illustrating from Fig.11 (a) - (c), the ZCS condition at the turn-off time can be discovered in the current of all diodes, which eliminates the reverse recovery loss. In addition, the maximum reverse voltages on the converter diodes are $V_{D1,2}=V_{Dc}=40$ V, $V_{D3}=90$ V, $V_{D4}=110$ V, and $V_{Do}=110$ V which are lower against the output voltage ($V_o=250$ V). Moreover, the current passed the output diode D_o turns-on and turns-off reaches zero under a very low slope (due to sinusoidal form). This leads to output voltage of the proposed converter, that is regulated without any spike and noise at the switching



(a)



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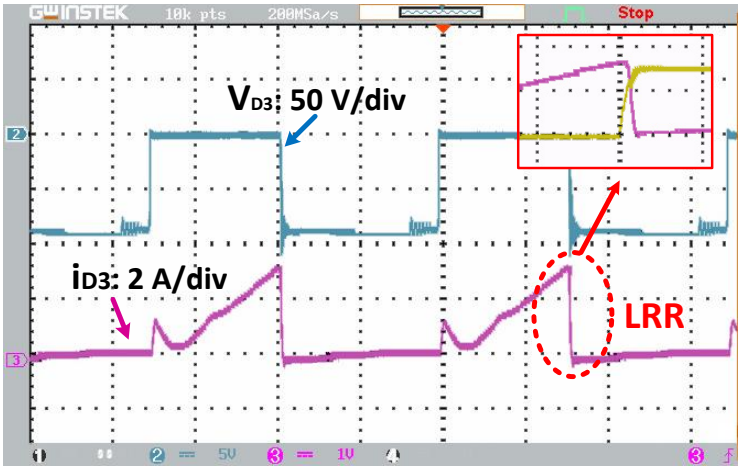

(c)

Fig. 11. Experimental results of the presented converter under the full-load of 160 W (LRR=Low Reverse Recovery), (a) The voltages and currents of the diodes Do and D1&2, (b) The voltages and currents of the diodes D4 and Dc, (c) The voltage and current of the diode D3.

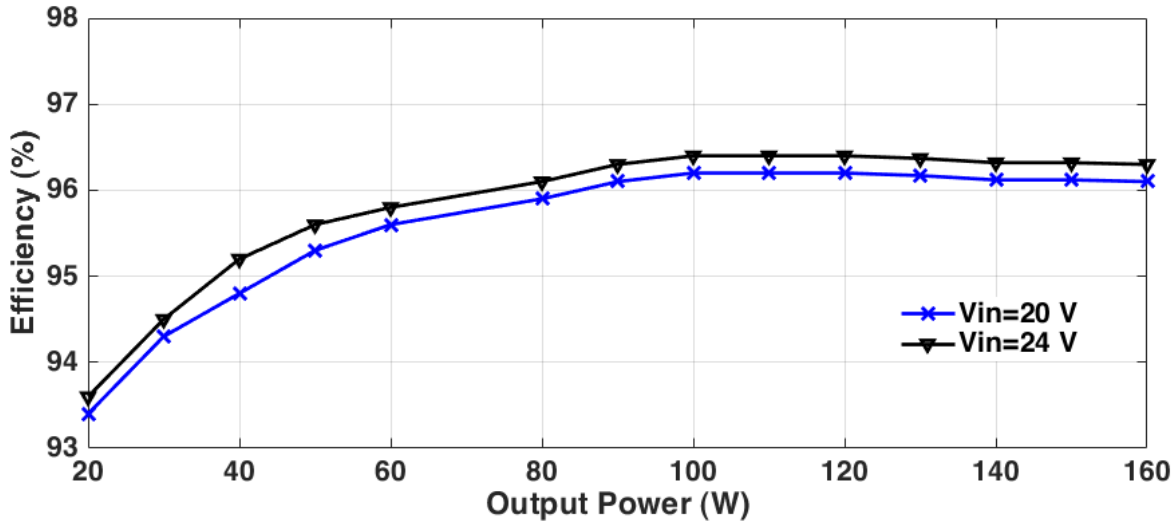

Fig. 12. Measured efficiencies of the proposed converter as a function of output powers.

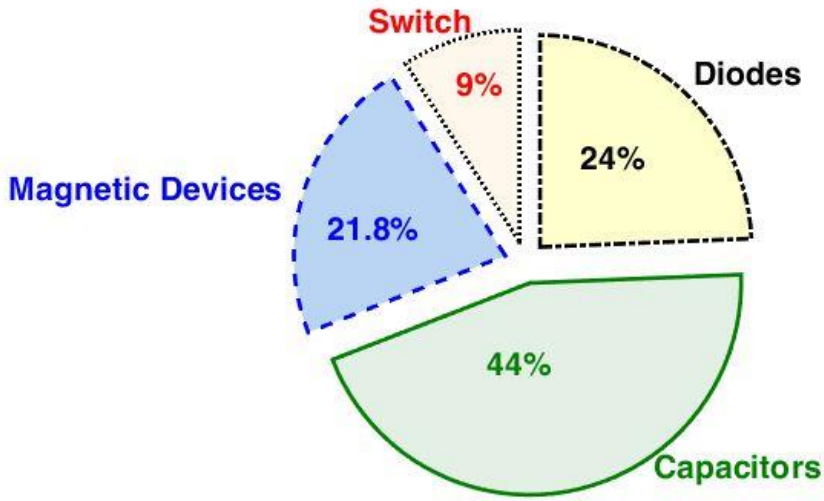

Fig. 13. Break-down of power dissipations of the proposed converter at full-load (P_{out} = 160 W).

instant, which is another advantage of the proposed topology.

Additionally, the practical efficiency of the converter as a function of the output power under the constant output voltage V_o= 250 V for two different input voltages V_{in}= 20 V and V_{in}= 24 V, is depicted in Fig. 12. The overall efficiency of the proposed converter at full-load condition (160 W) is about 96.3%. One can see that decreasing the voltage gain ratio can improve efficiency.

The breakdown of power dissipations of the presented converter at full-load condition (Table 2) is calculated as a pie graph, which is depicted in Fig. 13. The parasitic components of the converter devices are chosen according to datasheets. Due to low voltage stress and soft-switching operation, the power loss portion of the single power switch is low. A photograph of the proposed converter prototype is shown in Fig. 14.

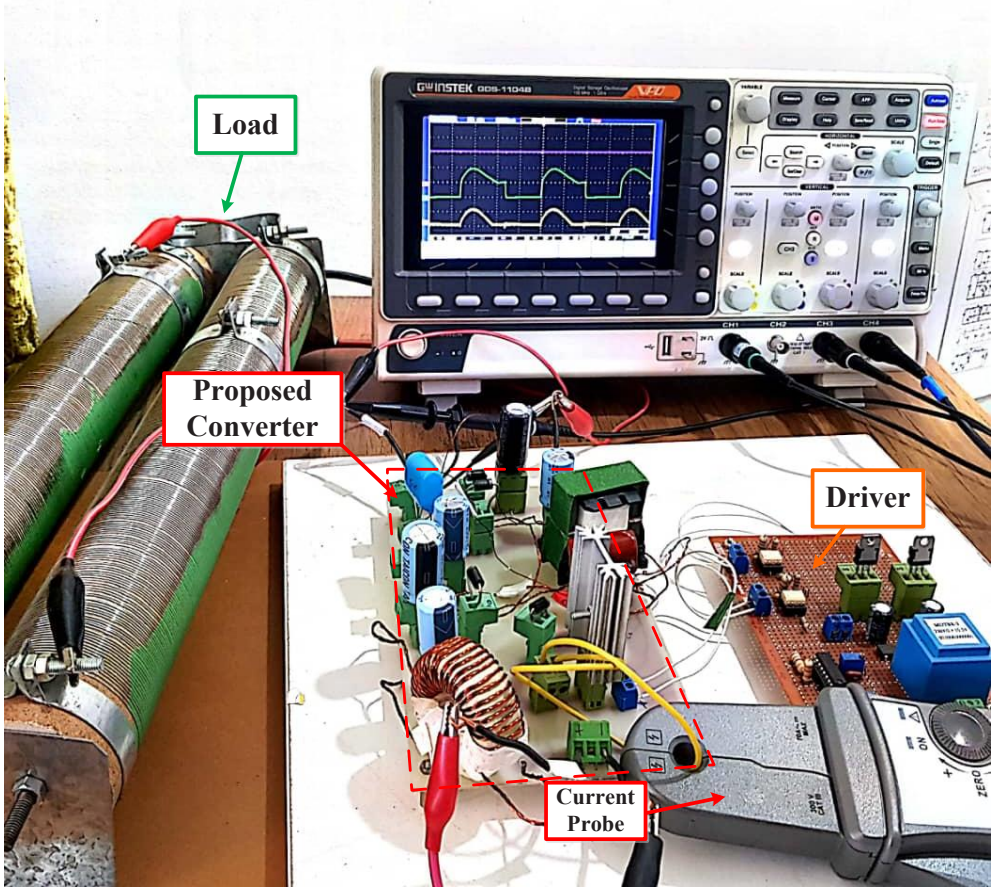

Fig. 14. A photograph of the laboratory prototype under test.

7- Conclusion

This paper presented a new single-switch ultra-step-up DC-DC converter using three winding coupled-inductor and two units of voltage multiplier. The experimental results are carried out on the laboratory prototype with 24 V input voltage and 250 V output voltage operating at 55 kHz. In practice, the proposed converter was able to provide a high voltage gain M=10.4) only using $n_{21}+n_{31}=1.5$ and a reasonable duty cycle (D=0.55). Regarding the experimental results, the input current passed through the input voltage source is continuous with a low ripple, which improves the lifetime of the renewable energy sources. In addition, the single power MOSFET turns on at ZCS condition with a low voltage stress $V_{DS} \approx 40$ V. Due to QR operation, the current value of the switch at turn-off instant is alleviated significantly ($i_{SW(t=off)} \approx 10$ A). Moreover, it was shown that the reverse recovery power losses of all the diodes in the circuit are very small. In addition, the maximum voltage stresses across all the diodes are lower than the output voltage, which reduces the losses of these diodes ($V_{D1,2}=V_{Dc}=40$ V, $V_{D3}=90$ V, $V_{D4}=110$ V, and $V_{Do}=110$ V). Additionally, Due to the soft switching performance in the proposed converter, the output voltage is obtained without any spike at the switching transitions. Moreover, the measured efficiency of the prototype was about 96.3% under the full-load condition. The experimental results demonstrated a good agreement with the theoretical analysis. The practical results clearly show all soft-switching points of the switching components, which justified the high-power conversion efficiency capability.

Nomenclature:

D	Duty cycle of the main switch
f_s	Switching frequency
f_R	Resonant frequency
LRR	Low Reverse Recovery
QR	Quasi-Resonant
RRP	Reverse Recovery Problem
TWCI	Three-Winding Coupled-Inductor
N_1, N_2, and N_3	Turn's ratio of the primary, secondary, and tertiary windings of the TWCI
SC	Switched-Capacitor
SI	Switched-Inductor
CI	Coupled-Inductor
VM	Voltage Multiplier
VMC	Voltage Multiplier Cell
VMR	Voltage Multiplier Rectifier
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition
3D	Three-Dimensional

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HOW TO CITE THIS ARTICLE

S. Hasanpour, M. Forouzesh, Y. P. Siwakoti, Full Soft-Switching Ultra-High Gain DC/DC Converter Using Three-Winding Coupled-Inductor with Modular Scalability for Renewable Energy Applications, AUT J. Elec. Eng., 54(1) (2022) 49-66.

DOI: 10.22060/eej.2021.20211.5423