



A New 13-Level Flying Capacitor-based 1- ϕ Inverter with Full Reactive Power Support

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ABSTRACT: This paper introduces a new symmetric single-phase 13-Level Flying Capacitor Inverter (13-LFCI) structure, using a two dc sources and three capacitors. The proposed single-phase 13-level inverter has the ability to increase the output voltage with fewer semiconductor components compared to the state-of-the-art structures. The Phase Disposition Sinusoidal Pulse Width Modulation (PDSPWM) method is utilized to produce switching pulses. Using this modulation scheme facilitate the 13-LFCI with self-balancing capacitors' voltage capability. The optimal capacitors are designed for minimum voltage drop in the different loads. The 13-LFCI is also capable of transferring reactive power through R-L loads without any limitations. Furthermore, the inverter can properly generate 5-level, 7-Level, 9-level, 11-level, and 13-level output voltage for different applications with change of modulation index. Moreover, a comparison with state-of-the-art 13-level inverters is provided in terms of the number of active and passive components, boosting ability, reactive power support and voltage conversion ratio in order to show the advantages of the proposed structure. In addition, the theoretically losses are calculated to show the efficiency of the proposed topology in various powers. The performance of the converter is illustrated through different operating conditions simulations of resistive and resistive-inductive loads. Eventually, to confirm different aspects and implementation of the proposed structure, the proposed 13-LFCI has been approved in MATLAB/SIMULINK software, and the achieved simulation results are considered utilizing a laboratory prototype.

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1- Introduction

Multi-Level Inverters (MLIs) have received more attention in the industry due to advantages such as low frequency modulation, high quality output waveform, high power performance, low electromagnetic interference and low harmonic distortion coefficient [1]. Basic MLI structures include diode clamp inverters, Flying Capacitor Multilevel Inverters (FCMIs), and Cascade Full Bridge Inverters (CFBIs). These inverters are used in expanded form to obtain a further number of voltage levels [2]. In these basic MLIs, the larger number of semiconductor devices and capacitors increases the power loss, cost and size of the converter [3]. Furthermore, grid connected multilevel inverters require extra DC-DC boost converters in renewable energy applications to preserve the dc link voltage. In these systems, boost circuits increase volume, size, cost and loss of converters [4].

Various structures have been introduced in order to solve these issues. A seven-level transformer-based inverter is presented in [5] for grid-tied applications. In [6], a single stage grid connected inverter is introduced without any DC-DC converter or transformer yielding low losses

and costs. Furthermore, in [7], a Y-source grid-connected inverter is presented for Photovoltaic (PV) applications with coupled inductor. Moreover, a transformer-less three-level flying capacitor grid-connected inverter is presented in [8] for renewable energy application with fewer number of components.

Nowadays, MLIs with low number of input sources, low number of semiconductor devices, and high efficiencies have gained increasing interest in order to overcome the structural issues of basic converters. Among these converters, the FCMIs have received more attention due to their voltage boosting capability without using additional circuits. Moreover, the voltage across capacitors is divided to produce multiple voltage steps at the output voltage [9] in these converters, which introduces lower harmonics. However, balancing the voltage of capacitors in FCMIs has become an important challenge in the practice. In some of the recently introduced topologies, this feature is performed with extra circuits, and in others, this aspect is guaranteed inherently due to the nature of the converter structure. For instance, a novel FCMI is presented in [10] which is equipped with an extra circuit to balance the voltage of capacitors. Another flying capacitor inverter is presented in [11] with voltage self-balancing

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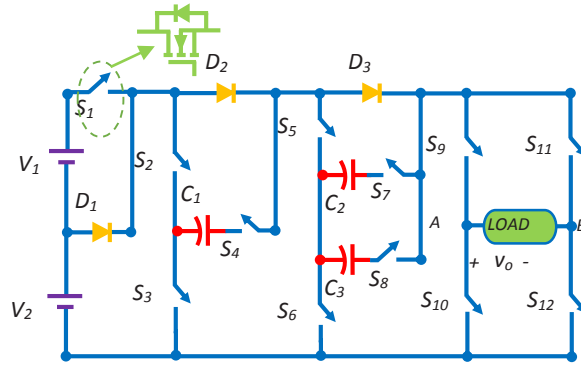


Fig. 1. The proposed 13-level flying capacitor-based inverter.

capability. This feature implies not only having simple circuit topology and lowest costs, but also results in simple controller and higher reliability. In addition, a single-phase FCMI with a unit output gain is presented in [12]. In this topology, the input voltage is divided among four capacitors and a nine-level voltage is generated at the output terminal. Additionally, changing of modulation index generates different output voltages in FCMI for different applications. Moreover, the number of output voltage levels in [13] has been changed by adjusting of modulation indices, hence the Total Harmonic Distortion (THD) of voltage is maintained to a minimum value at different conditions. All the multilevel inverters have full reactive power capability for current paths in the resistive-inductive loads. This limitation is due to the circuit arrangement of topology [14].

This paper introduces a new 1 ϕ -13-level based symmetric flying capacitor inverter topology with voltage boosting and capacitor voltage balancing capabilities. This feature decreases the control intricacy without extra sensor. The proposed structure generates a boosted output voltage without using the inductor or transformer. The output THD of voltage is also degraded by employing the PDSPWM method. This paper is formed as follows: the proposed new SMFCI structure and operation modes are presented in section 2. In addition, the optimal capacitor design is explained in section 3. Additionally, the calculations of power losses in the proposed 13-LFCI are clarified in section 4. In section 5 a comparison study of the proposed 13-LFCI with other similar topologies is provided. The simulation and hardware results illustrating the performance of the presented structure are presented in section 6 and section 7. Finally, the paper is summarized in section 8.

2- Proposed 13-level Flying Capacitor Inverter

This section will present the circuit topology, operation modes and modulation strategy of the suggested structure in the following.

2- 1- Proposed Circuit Topology

The proposed single phase 13-level flying capacitor

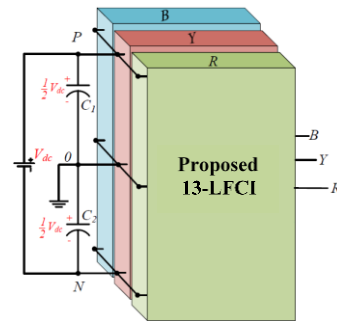


Fig. 2. The configuration circuit of the 3- ϕ proposed 13-LFCI inverter.

inverter circuit is shown in Fig. 1. This structure uses the H-Bridge part to generate negative and positive waveforms of the output voltage. The proposed topology includes two dc input voltage sources ($V_1=V_{dc}$, $V_2=V_{dc}$), three fast recovery diodes (D_1 - D_3), three dc capacitors (C_1 - C_3) and twelve power switches (S_1 - S_{12}). The operation of the proposed inverter is specified in the following:

The proposed inverter can be extended to the three-phase multilevel inverter. To do so, the two input dc sources can be replaced with two capacitors in each phase, leg of proposed topology with only dc power sources based on neutral point clamped inverter as shown in Fig. 2. A configuration circuit of the 3- ϕ proposed inverter with its related voltage of phase and related voltage of line is demonstrated in Fig. 2.

2- 2- Switching Modes

The equivalent circuit of the suggested 13-LFCI is shown in Fig. 3. The switching modes of the structure consist of fourteen states. Due to symmetry in the operation modes, only the positive half cycle of produced operational modes are discussed as follows:

Mode I) $V_{AB} = 0^+$: As depicted in Fig. 3 (a), to generate a zero-output level, the switches S_9 and S_{11} are ON in the

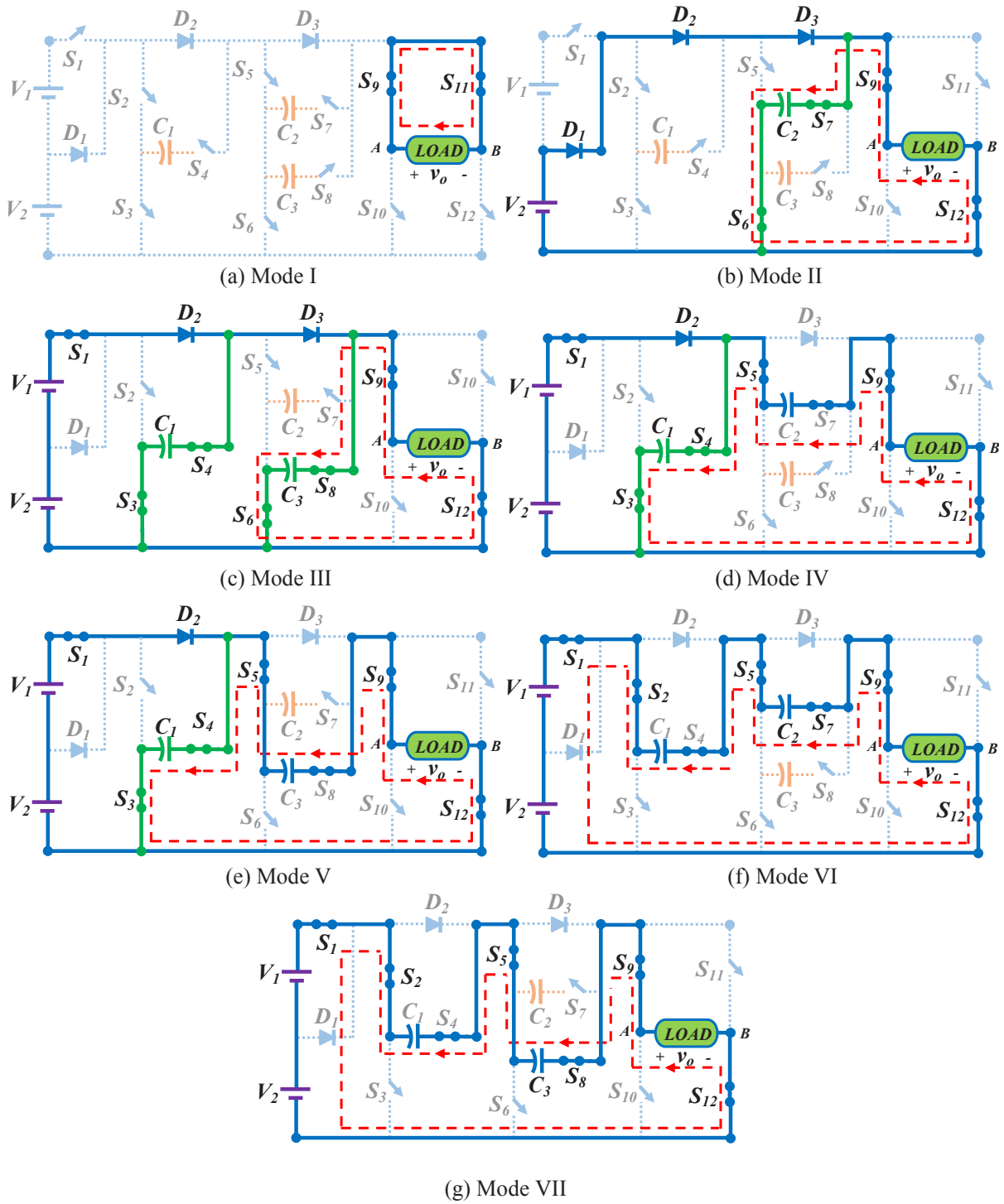


Fig. 3. Switching states and conduction paths of the proposed 13-LFCI: (a) Mode I ($V_{AB} = 0+$), (b) Mode II ($V_{AB} = V_{dc}$), (c) Mode III ($V_{AB} = 2V_{dc}$), (d) Mode IV ($V_{AB} = 3V_{dc}$), (e) Mode V ($V_{AB} = 4V_{dc}$), (f) Mode VI ($V_{AB} = 5V_{dc}$), (g) Mode VII ($V_{AB} = 6V_{dc}$).

Table 1. Charging and discharging pattern of capacitors in different switching modes (▲: charging, ▼ : discharging).

Mode	V _{AB}	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁	S ₁₂	C ₁	C ₂	C ₃
I	0 ⁺	0	0	0	0	0	0	0	0	1	0	1	0	--	--	--
II	V _{dc}	0	0	0	0	0	1	1	0	1	0	0	1	--	▲	--
III	2V _{dc}	1	0	1	1	0	1	0	1	1	0	0	1	▲	--	▲
IV	3V _{dc}	1	0	1	1	1	0	1	0	1	0	0	1	▲	▼	
V	4V _{dc}	1	0	1	1	1	0	0	1	1	0	0	1	▲	--	▼
VI	5V _{dc}	1	1	0	1	1	0	1	0	1	0	0	1	▼	▼	
VII	6V _{dc}	1	1	0	1	1	0	0	1	1	0	0	1	▼	--	▼
VIII	0 ⁻	0	0	0	0	0	0	0	0	0	1	0	1	--	--	--
IX	-V _{dc}	0	0	0	0	0	1	1	0	0	1	1	0	--	▲	--
X	-2V _{dc}	1	0	1	1	0	1	0	1	0	1	1	0	▲	--	▲
XI	-3V _{dc}	1	0	1	1	1	0	1	0	0	1	1	0	▲	▼	--
XII	-4V _{dc}	1	0	1	1	1	0	0	1	0	1	1	0	▲	--	▼
XIII	-5V _{dc}	1	1	0	1	1	0	1	0	0	1	1	0	▼	▼	--
XIV	-6V _{dc}	1	1	0	1	1	0	0	1	0	1	1	0	▼	--	▼

positive half cycle. Mode II) $V_{AB} = V_2$: According to Fig. 3 (b), the diodes D_1 , D_2 and D_3 are in forward bias mode and the switches S_6 , S_7 , S_9 and S_{12} are ON. It is clear that the capacitor C_2 is charged in parallel with the voltage source V_2 . Mode III) $V_{AB} = V_1 + V_2$: As shown in Fig. 3 (c), in this operational mode S_1 , S_3 , S_4 , S_6 , S_8 , S_9 and S_{12} are ON and the diodes D_2 and D_3 are in forward bias mode to generate third level output voltage. Two capacitors C_1 and C_3 are charged in parallel with sum of the input voltage sources V_1 and V_2 . Mode IV) $V_{AB} = V_1 + V_2 + V_{C2}$: In this operation mode which is depicted in Fig. 3 (d), the switches S_1 , S_3 , S_4 , S_5 , S_9 and S_{12} are ON and capacitor C_2 is discharged but the capacitor C_1 is charged in series connection with sum of the input voltage sources. Mode V) $V_{AB} = V_1 + V_2 + V_{C3}$: As shown in Fig. 3 (e), to generate five output voltage levels, the switches S_1 , S_3 , S_4 , S_5 , S_8 , S_9 and S_{12} are ON and the capacitor C_3 is discharged but the capacitor C_1 is charged in series connection with sum of input voltage sources. Mode VI) $V_{AB} = V_1 + V_2 + V_{C1} + V_{C2}$: The switches S_1 , S_2 , S_4 , S_5 , S_7 , S_9 and S_{12} are ON and the capacitors C_1 and C_2 are discharged in the series connection with the input voltage sources according to Fig. 3 (f). Mode VII) $V_{AB} = V_1 + V_2 + V_{C1} + V_{C3}$: As shown in Fig. 3 (g), S_1 , S_2 , S_4 , S_5 , S_8 , S_9 and S_{12} are ON. To generate the fourth level, the capacitors C_1 and C_3 are connected in series with the input voltage sources.

The switching modes, the charging and discharging times of each capacitor in different operating modes of the proposed 13-LFCI are summarized in Table 1. In all modes, all capacitors charged in parallel and discharged in series with the input voltage sources. As depicted in Fig. 4, the waveform of 13-level output voltage has been produced by comparing the reference waveform with the six-carrier signal using PDSPWM technique.

3- Optimal Sizing of Capacitors in the Proposed 13-LFCI

In order to achieve minimum voltage ripple of capacitor voltage and also reduce the capacitors size, the optimal capacitance of the capacitors is an important challenge in FC inverters. The voltage drop of the capacitors occurs during discharge mode. The maximum discharge time of the capacitors in an alternating period is studied to determine the optimal capacitance. The amount of electric charge of each capacitor during discharge time is obtained by using (1) in the proposed 13-LFCI [15].

$$Q_{C,i} = \int_{t_k}^{t_p} i_{C,i}(t) dt \quad (1)$$

Where the time period of (1) shows the discharging time of the capacitor C_i and $i_{C,i}$ is the current passing through the capacitor. According to operation modes, output current equals to $i_{C,i}$ due to the discharging modes which is obtained as:

$$i_{C,i}(t) = i_o(t) = i_m \sin \omega t \quad (2)$$

Where, i_m is the maximum load current. By combining equations (1) and (2), the optimal capacitance can be obtained by using (3) as:

$$C_{Op,i} \geq \frac{\int_{t_k}^{t_p} i_{C,i}(t) dt}{\Delta V_{C_i}} \quad \forall i = 1, 2, 3 \quad (3)$$

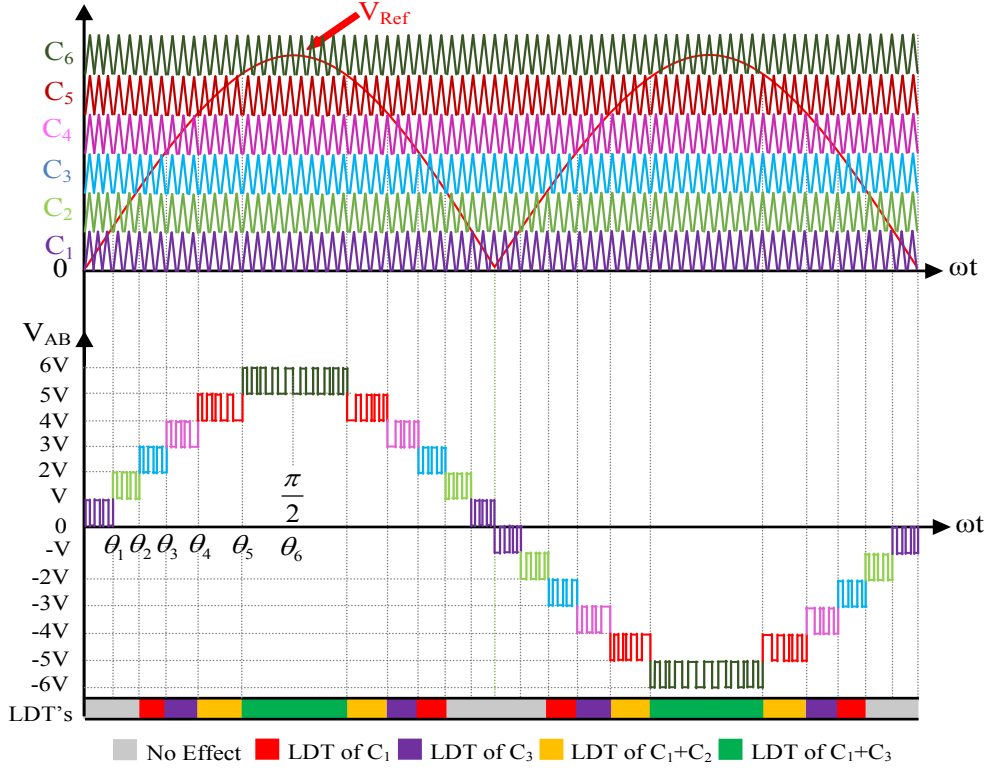


Fig. 4. Modulation scheme of the proposed 13-LFCI, switching pattern and output voltage waveform.

Where, ΔV_{C_i} is the maximum voltage ripple of the capacitors. By considering different load resistor and Large Discharge Time (LDT) of three capacitors of the proposed 13-LFCI (LDT_1 , LDT_2 , LDT_3) according to Fig. 4, the optimal capacitance of each capacitor for different voltage ripple are depicted in Fig. 5.

3- 1- Calculations of Power Losses in the Proposed 13-LFCI

The power losses for a proposed 13-LFCI is combined of three sections involving $P_{Switching}$, $P_{Conduction}$, and P_{Ripple} [16], which are described with detail according to the following:

3- 1- 1- Calculation of Switching Losses (P_{sw})

The switching losses happen during turning-on or turning-off time due to the energy saving in the output capacitance of each switch [16]. This energy is obtained for near output levels in the proposed 13-LFCI as follows:

$$\begin{cases} E_{(+0 \leftrightarrow +V_{dc})} = E_{(-0 \leftrightarrow -V_{dc})} = C_s (V_{dc})^2 \\ E_{(+V_{dc} \leftrightarrow +2V_{dc})} = E_{(-V_{dc} \leftrightarrow -2V_{dc})} = C_s (V_{dc})^2 \\ E_{(+2V_{dc} \leftrightarrow +3V_{dc})} = E_{(-2V_{dc} \leftrightarrow -3V_{dc})} = C_s (V_{dc})^2 + C_s (2V_{dc})^2 \\ E_{(+3V_{dc} \leftrightarrow +4V_{dc})} = E_{(-3V_{dc} \leftrightarrow -4V_{dc})} = 2C_s (V_{dc})^2 \\ E_{(+4V_{dc} \leftrightarrow +5V_{dc})} = E_{(-4V_{dc} \leftrightarrow -5V_{dc})} = 2C_s (V_{dc})^2 + C_s (2V_{dc})^2 \\ E_{(+5V_{dc} \leftrightarrow +6V_{dc})} = E_{(-5V_{dc} \leftrightarrow -6V_{dc})} = 2C_s (V_{dc})^2 \end{cases} \quad (4)$$

In (4), C_s denotes the output capacitance of switches. Additionally, the duration of switching between two near output levels ($t_{L_i \leftrightarrow L_{i+1}}$) in the proposed 13-LFCI will be as follows:

$$\begin{cases} t_{(+0 \leftrightarrow +V_{dc})} = t_{(-0 \leftrightarrow -V_{dc})} = (f_s / \pi) \times (\theta_1 - 0) \\ t_{(+V_{dc} \leftrightarrow +2V_{dc})} = t_{(-V_{dc} \leftrightarrow -2V_{dc})} = (f_s / \pi) \times (\theta_2 - \theta_1) \\ t_{(+2V_{dc} \leftrightarrow +3V_{dc})} = t_{(-2V_{dc} \leftrightarrow -3V_{dc})} = (f_s / \pi) \times (\theta_3 - \theta_2) \\ t_{(+3V_{dc} \leftrightarrow +4V_{dc})} = t_{(-3V_{dc} \leftrightarrow -4V_{dc})} = (f_s / \pi) \times (\theta_4 - \theta_3) \\ t_{(+4V_{dc} \leftrightarrow +5V_{dc})} = t_{(-4V_{dc} \leftrightarrow -5V_{dc})} = (f_s / \pi) \times (\theta_5 - \theta_4) \\ t_{(+5V_{dc} \leftrightarrow +6V_{dc})} = t_{(-5V_{dc} \leftrightarrow -6V_{dc})} = (f_s / \pi) \times (\pi/2 - \theta_5) \end{cases} \quad (5)$$

where f_s is the switching frequency, and θ_i is the switching angles in different levels according to Fig. 4. The following equation explains the whole switching losses in the proposed topology [16].

$$P_{SW,T} = 4 \sum_{i=0}^5 (E_{(L_i \leftrightarrow L_{i+1})} \times t_{(L_i \leftrightarrow L_{i+1})}) \quad (6)$$

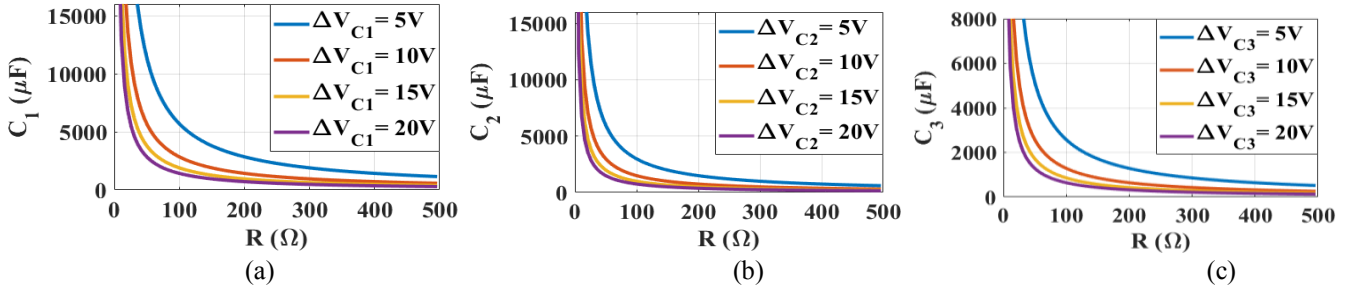


Fig. 5. Changes of optimal capacitors against RL for (a) C1, (b) C2 and (c) C3.

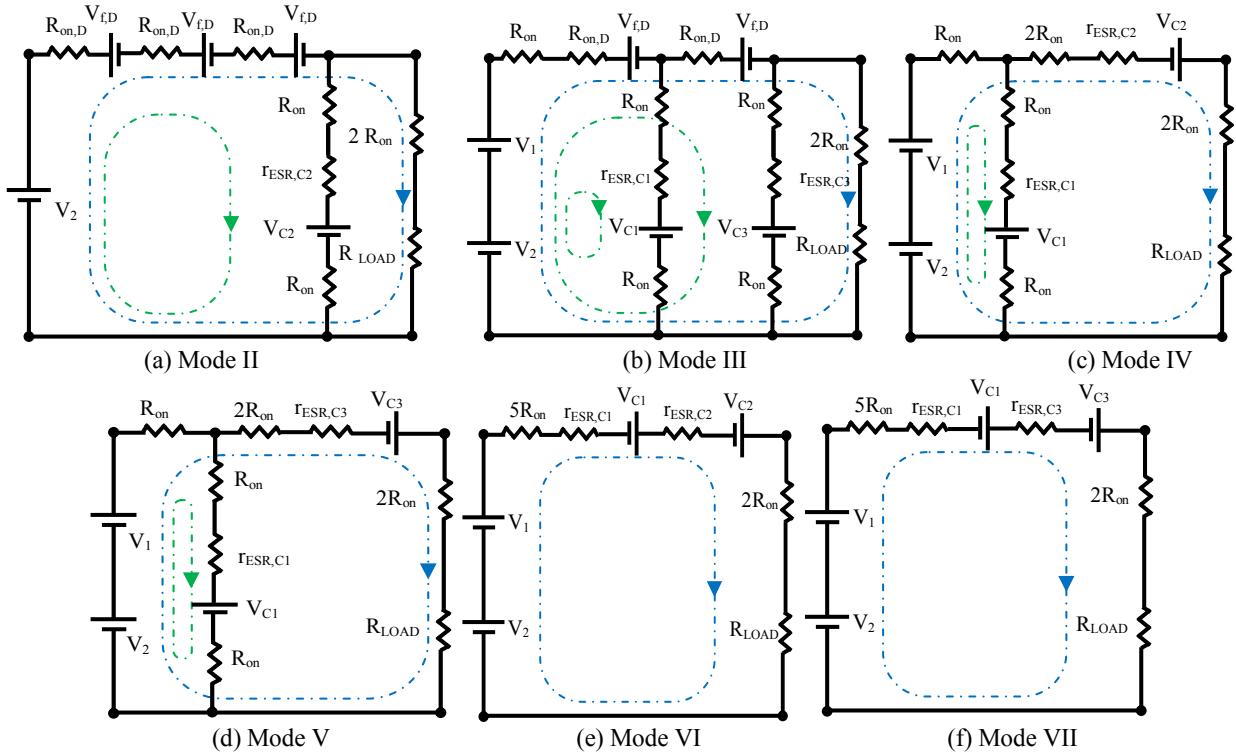


Fig. 6. The equivalent load current and charging path of proposed 13-LFCI for positive half period in (a) Mode II, (b) Mode III, (c) Mode IV, (d) Mode V, (d) Mode VI, (d) Mode VII.

3- 1- 2- Calculation of Conducting Losses (P_c)

The conduction losses in the proposed inverter are entirely due to the parasitic elements. As shown in Fig. 5, the load current path (blue dashed line) and charging current path (green dashed line) are shown in the equivalent configuration of the proposed 13-LFCI based on operation modes according to Fig. 3. The whole parasitic resistances in the output current path are calculated as (7) [16] at positive operation states according to Fig. 6.

$$\begin{cases} R_{(eq,+v_{dc})} = 3R_{on,D} + 2R_{on} \\ R_{(eq,+2v_{dc})} = 2R_{on,D} + 3R_{on} \\ R_{(eq,+3v_{dc})} = 5R_{on} + r_{ESR-C_2} \\ R_{(eq,+4v_{dc})} = 5R_{on} + r_{ESR-C_3} \\ R_{(eq,+5v_{dc})} = 7R_{on} + r_{ESR-C_1} + r_{ESR-C_2} \\ R_{(eq,+6v_{dc})} = 7R_{on} + r_{ESR-C_1} + r_{ESR-C_3} \end{cases} \quad (7)$$

Table 2. Table of used elements in the power losses.

Element	Value	Element	Value
DC Voltage (V_{dc})	100V	C_1	Capacitance = 1400 μ F, $r_{ESR} = 270 \text{ m}\Omega$
MOSFET (STW20NM60FD)	$C_s = 500 \text{ pF}$ $R_{ON} = 0.29 \Omega$	C_2	Capacitance = 1000 μ F, $r_{ESR} = 112 \text{ m}\Omega$
DIODE (C3D10060A)	$R_{onD} = 6\text{m}\Omega$ $V_{fD} = 1.5\text{V}$	C_3	Capacitance = 1000 μ F, $r_{ESR} = 112 \text{ m}\Omega$

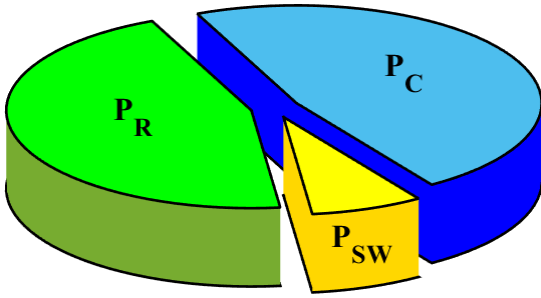


Fig. 7. Distribution of power losses at 600W.

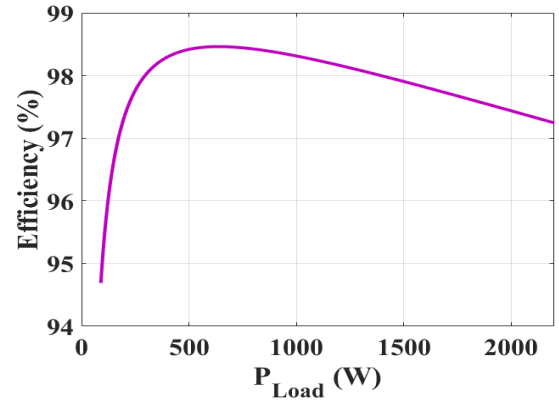


Fig. 8. Proposed 13-LFCI efficiency curve.

Where $R_{(eq,i-v_{dc})}$ is the whole parasitic resistance in output current path at i -level. R_{onD} , R_{on} , and r_{ESR-C} are the series resistance of each diode and the internal resistance of switch and internal resistance of each capacitor, respectively.

Considering Fig. 6, the load current can be written as:

$$\begin{cases} I_{L,1} = (V_{dc} - 3V_{fD}) / (R_{(eq,+v_{dc})} + R_L) \\ I_{L,2} = 2V_{dc} - 2V_{fD} / (R_{(eq,+2v_{dc})} + R_L) \\ I_{L,3} = (2V_{dc} - V_{C2}) / (R_{(eq,+3v_{dc})} + R_L) \\ I_{L,4} = (2V_{dc} - V_{C3}) / (R_{(eq,+4v_{dc})} + R_L) \\ I_{L,5} = (2V_{dc} + V_{C1} + V_{C2}) / (R_{(eq,+5v_{dc})} + R_L) \\ I_{L,6} = (2V_{dc} + V_{C1} + V_{C3}) / (R_{(eq,+6v_{dc})} + R_L) \end{cases} \quad (8)$$

The following equation explains the whole conduction losses in the proposed topology.

$$P_{C,T} = 4f_o \sum_{i=0}^5 \left((I_{L,i+1})^2 \int_{\theta_i/\omega}^{\theta_{(i+1)}/\omega} R_{(eq,(i+1)v_{dc})} \sin(\omega t) dt \right) \quad (9)$$

Where f_o is load frequency.

3- 1- 3- Calculation of Capacitor Ripple Losses (P_R) [16]

All the ripple losses on the capacitors for proposed inverter can be calculated by:

$$P_{R,T} = f_o \sum_{i=1}^3 C_i \left(\int_{\alpha_i/\omega}^{\alpha'_i/\omega} i_{Ci}(t) dt \right)^2 \quad (10)$$

where $i_{ci}(t)$ is the capacitors' current according to green dashed lines of Fig. 6, and $[\alpha'_i - \alpha_i]$ is ascribed time to charging states of capacitors according to Fig. 4.

The different sections of power losses for proposed 13-LFCI is computed by MATLAB at 600W according to Fig. 7. The used parameters are listed in Table 2. Methodical efficiency curve of the proposed 13-LFCI is demonstrated in Fig. 8 at various load power. As observed in this curve, the efficiency is 98.45% at 600W.

4- Comparison Study

The comparisons of the proposed 13-LFCI with some similar topologies are summarized in Table 3. This comparison is presented with respect to the number of dc sources (N_{DC}), number of switches (N_s), number of diodes (N_D), number of capacitors (N_C), Boosting Ability (BA), Voltage Conversion Ratio (VCR), and Reactive Power Support (RPS). All these FCMLIs produce thirteen output levels and these topologies

Table 3. Comparison of the proposed 13-LFCI with similar 13-level FCMLIs.

Parameters	N _{DC}	N _S	N _D	N _C	BA	VCR	RPS
[17]	2	20	0	6	Yes	1.5	YES
[18]	2	18	2	4	Yes	3	YES
[19]	2	16	2	4	Yes	3	YES
[20]	2	16	4	4	Yes	3	YES
Proposed 13-LFCI	2	12	3	3	Yes	3	YES

Table 4. Comparison of the proposed three-phase inverter with other structures.

Parameters	No of whole switching devices	No of gate driver	No of power sources or capacitors	No of levels in the phase voltage
[21]	24	24	2	11
[22]	24	24	6	7
[23]	42	42	15	9
[24]	18	18	9	5
[25]	24	24	12	5
Proposed topology	51	51	18	13

use two dc power voltage sources. Based on this table, the comparison shows the proposed 13-LFCI gets better achievement in terms of number of total passive components. From the aspect of N_S, the proposed 13-LFCI has a smaller number of switches compared to other suggested topologies. It is clear that using more power switches reduces system efficiency and reliability as well as increases the system size and cost due to high number of switches and corresponding cooling system. Therefore, the proposed structure introduces lower power loss and costs compared to the similar topologies. Moreover, the boosting factor is the lowest in [17], but the other compared topologies have the equal boost ratios. Furthermore, the number of capacitors in proposed inverter is less than compared to other structures, and hence this result in rising the capacitance losses. The voltage conversion ratio of proposed 13-LFCI shows the boosting capability without any step-up converter similar to the other compared topologies. The suggested topology has full reactive power support for R-L loads. Furthermore, it is necessary to consider the proposed three-phase inverter with other three-phase topologies detailed in Table 4 to prove its performance. According to Table 4, various terms are considered, such as: number of whole switching components, number of drivers, number of power sources or capacitors, and number of levels in the line voltage. It is noted that the proposed inverter gets a greater number of levels in the line voltage with compared other topologies, but proposed topology is used higher number of switching devices.

5- Simulation Results

The proposed 13-LFCI is simulated in MATLAB/SIMULINK to validate its performance under resistive (R) and resistive-inductive (R-L) loading conditions. The input sources voltage in the proposed inverter is selected as 100V. Table 5 summarizes the proposed simulation parameters.

Fig. 9 illustrates the waveforms of the load current ($i_{AB(t)}$) and output voltage ($V_{AB(t)}$) with a resistance and R-L loads for step-change in load from R=300Ω to Z=300Ω+500mH. Voltage waveform, shown in Fig. 9, is made up of 13-levels with maximum amplitude of the voltage 600[V] without any variation in step change, and current changes from maximum 2[A] under pure resistive load to maximum 1.8[A] under RL load. These output voltage and output current are obtained with PDSPWM controlling strategy. According to this result, the voltage has gained three in the presented topology. According to Fig. 9, the sinusoidal current has a phase difference between the 13-level output voltage that shows the reactive power supporting capability of the proposed inverter. As it can be observed in Fig. 9, the phase difference is nearly 28° (φ), according to the applied RL condition. Fig. 10 and Fig. 11 demonstrate the output voltage and current waveforms under different RL load and different purely R loads, respectively.

The natural balancing of the capacitors for resistive load of 300Ω is demonstrated in Fig. 12 and Fig. 13. The voltage of the capacitors is boosted. According to Fig. 6, the voltage ripple of capacitors is approximately within 5V. Fig.

Table 5. The proposed 13-LFCI simulation parameters.

Components	Attributes
Input Voltages	$V_1 = 100$ [V], $V_2 = 100$ [V]
Max. Output Voltage	600 [V]
Capacitors [uF]	$C_1 = 1900$, $C_2 = 1000$, $C_3 = 850$
Switching Frequency	$f_{sw} = 25$ [kHz]
Reference Frequency	$f_{ref} = 50$ [Hz]

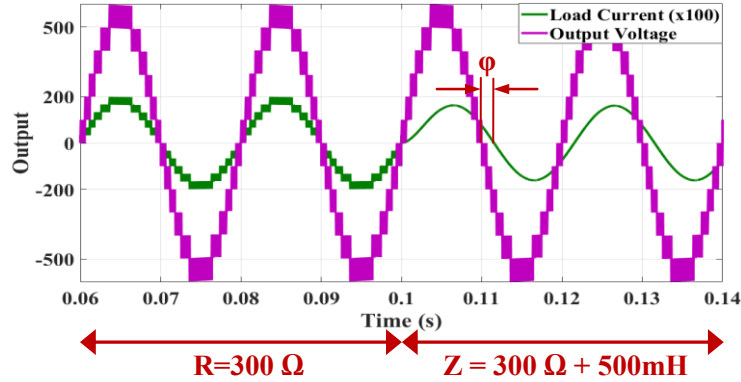


Fig. 9. The Output voltage and current of proposed 13-LFCI under change of load from R load to RL load.

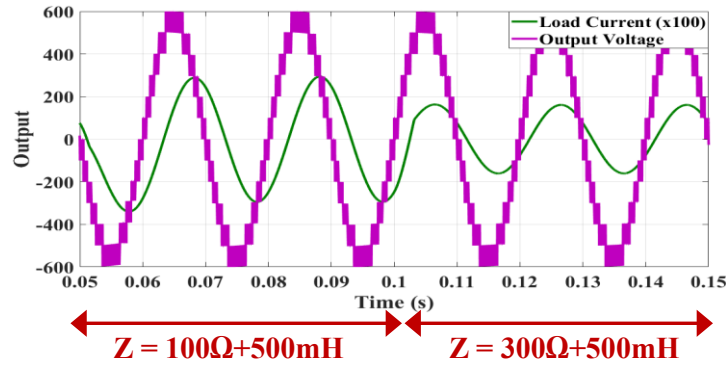


Fig. 10. The Output voltage and current of proposed 13-LFCI under change of load from different RL loads.

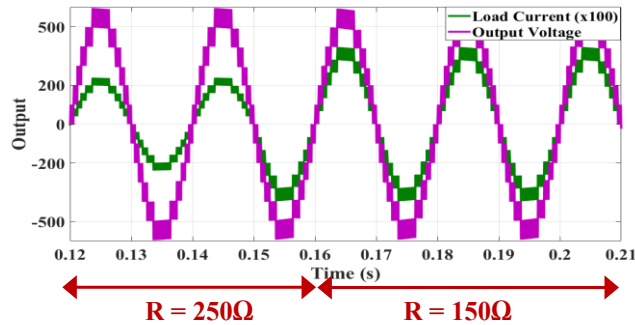


Fig. 11. The Output voltage and current of proposed 13-LFCI under change of load from $R=250\ \Omega$ to $R=150\ \Omega$ under RL load.

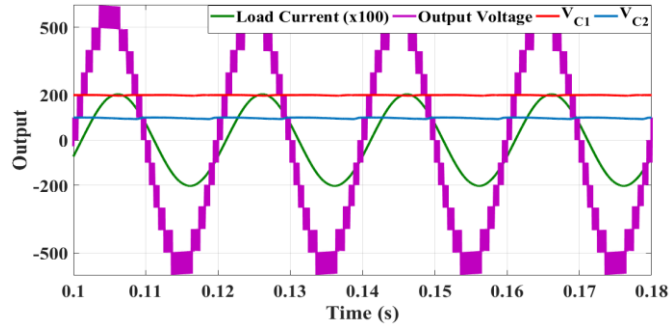


Fig. 12. The Output voltage and current of proposed 13-LFCI with capacitors voltage of C1 and C2 under resistive load

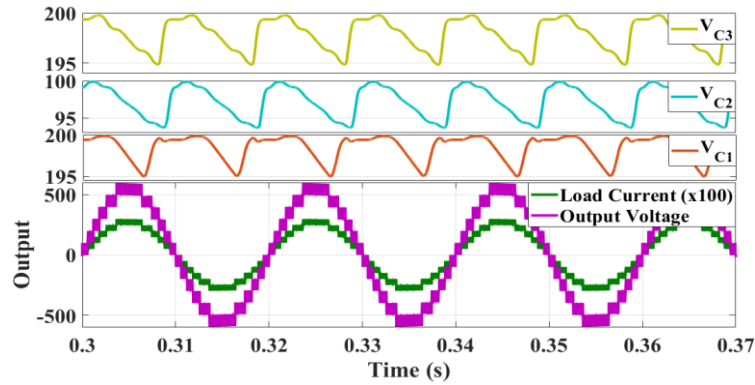


Fig. 13. The Output voltage and current of proposed 13-LFCI with voltage drop across C1, C2 and C3 under purely resistive load.

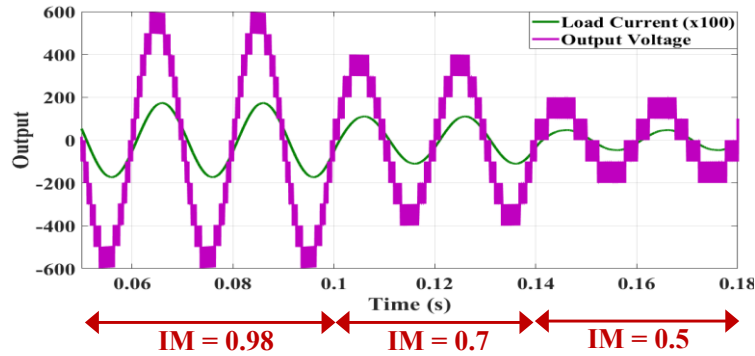


Fig. 14. The Output voltage and current of proposed 13-LFCI under change of index modulation.

14 depicts the simulation waveform for various modulation indices from 0.98 to 0.7, and then to 0.5. According to these figures, when $M_a = 0.5$, $M_a = 0.6$, $M_a = 0.7$ and $M_a = 0.8$, the proposed inverter generates eleven-level, nine-level, five-level of output voltage, respectively. This result shows that the output voltage levels of the proposed inverter changed with different modulation indexes.

It can be seen in Fig. 15 (a) and (b) that the output voltage THD at $M = 0.8$ and at $M = 0.6$ with PDSPWM technique are

7.8% and 13.14%, respectively. It can clearly be demonstrated that the voltage THD is increasing with reducing of modulation index. According to Fig. 15 (c), the THD of output current without any filters is 0.69% for resistive load of 300Ω and $M = 1$. Fig. 16 demonstrates the voltage waveforms across some switches of the presented flying capacitor inverter. The highest voltage stress of the presented FC inverter is related to the H-Bridge side switches (S_9 - S_{12}). Moreover, the currents of the input voltage sources are depicted in Fig. 16 (m) and Fig.

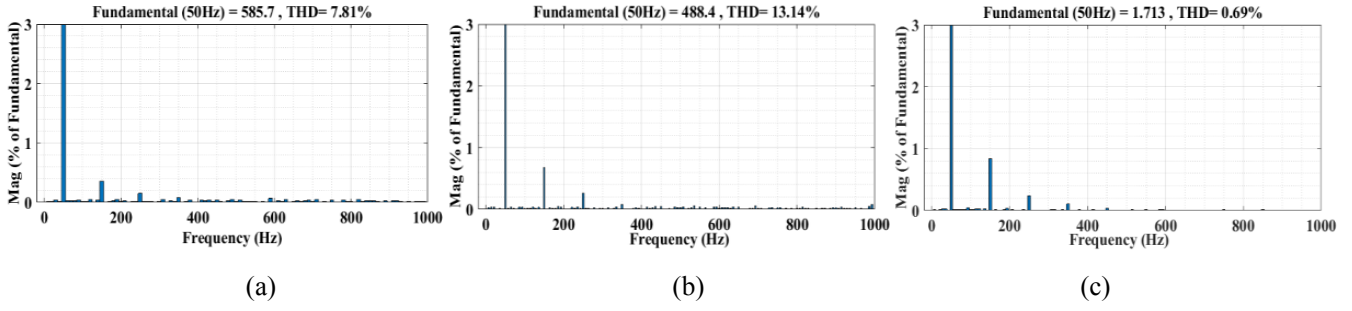


Fig. 15. Harmonic spectrum and THD of output voltage for a) resistive load of $300\ \Omega$ and $M = 0.8$ (11-Level), b) resistive load of $300\ \Omega$ and $M = 0.6$ (7-Level), c) harmonic spectrum and THD of output current for resistive load of $300\ \Omega$ and $M = 1$ (13-Level).

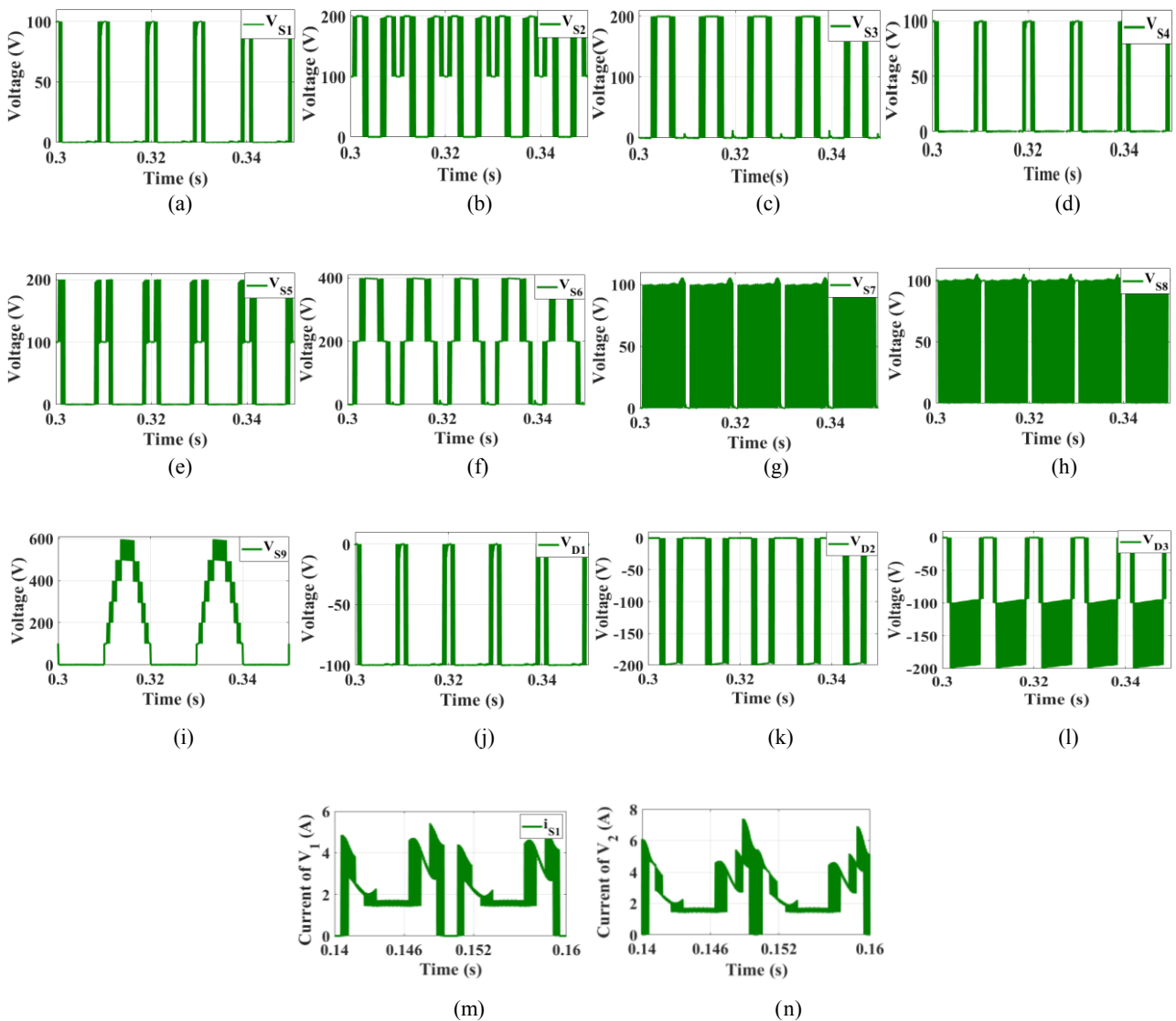


Fig. 16. Simulation results of voltage stress of (a) VS1, (b) VS2, (c) VS3, (d) VS4, (e) VS5, (f) VS6, (g) VS7, (h) VS8, (i) VS9, (j) VD1, (k) VD2, (l) VD3, (m) i_{S1} , (n) i_{S2} .

Table 6. The parameters values of laboratory setup

Parameters	Value
Input Voltages	$V_1 = 50$ [V], $V_2 = 50$ [V]
Capacitors [μ F]	$C_1 = 2000$, $C_2 = 1000$, $C_3 = 2000$
Switching Frequency	$f_{sw} = 10$ [kHz]
RL Load	60 [Ω], 200 [mH]
Output Power	500 VA
Gate drives	TLP 350

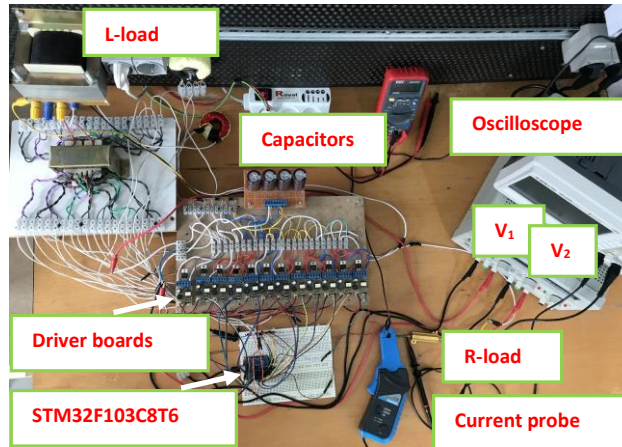


Fig. 17. Picture of the hardware set up.

16 (n) for resistive load of 300 Ω .

6- Hardware Results

A 500 VA experimental set up of proposed 13-LFCI has been assessed in the laboratory as demonstrated in Fig. 17. STM32F103C8T6 is utilized to produce the control signals. Two separate dc voltage sources are employed. The other components utilized in the laboratory setup are shown in Table 6. Fig. 18 (a) depicts the load voltage and load current waveforms for a R-L load of $Z = 60 \Omega + 200 \text{ mH}$. The 0.7 lagging power factor ($\varphi = -45^\circ$) is shown in Fig. 18 (a) according to the above loading condition. Furthermore, the thirteen distinctive load voltage has a maximum voltage of 300 V with a same voltage step of 50 V, and output current is sinusoidal. Additionally, Figure 18 (b), (c), and (d) demonstrate the voltage stress waveforms across some power switches in the proposed topology. It can be specified that the simulation and laboratory results of the voltage stress on power switches are similar with high accuracy. Fig. 18 (e) and Fig. 18 (f) demonstrate the harmonic spectrum of load voltage and load current respectively with switching frequency of 10 kHz. According to these experimental results the THD of load

voltage and load current are about 3% and 2.4% respectively. Eventually, the voltage across capacitors have been shown in Fig. 18 (g), (h), and (i) by considering 15 V ripple. According to the optimal sizing of capacitors in the proposed 13-LFCI in Fig. 4, the laboratory value of 2000 μ F and 1000 μ F are chosen for the C_1 and C_2 . The capacitance of C_1 and C_3 are same.

7- Conclusion

In this paper, a novel 13-level symmetric flying capacitor based single-phase inverter structure was proposed. The output voltage of the presented 13-level topology has two voltage sources with boosting capability. The voltage amplitude three times was gain of proposed 13-LFCI. The polarity of the output voltage was changed through H-Bridge on the output side of the proposed 13-LFCI. Moreover, the PDSPWM method has been used to generate pulses to obtain capacitors self-balancing capability without utilizing the complicated balance circuits or complex control methods. The proposed 13-LFCI has merits such as fewer voltage sources, boosting capability, and full reactive power transmission. The operational modes detail of 13-LFCI were introduced. The

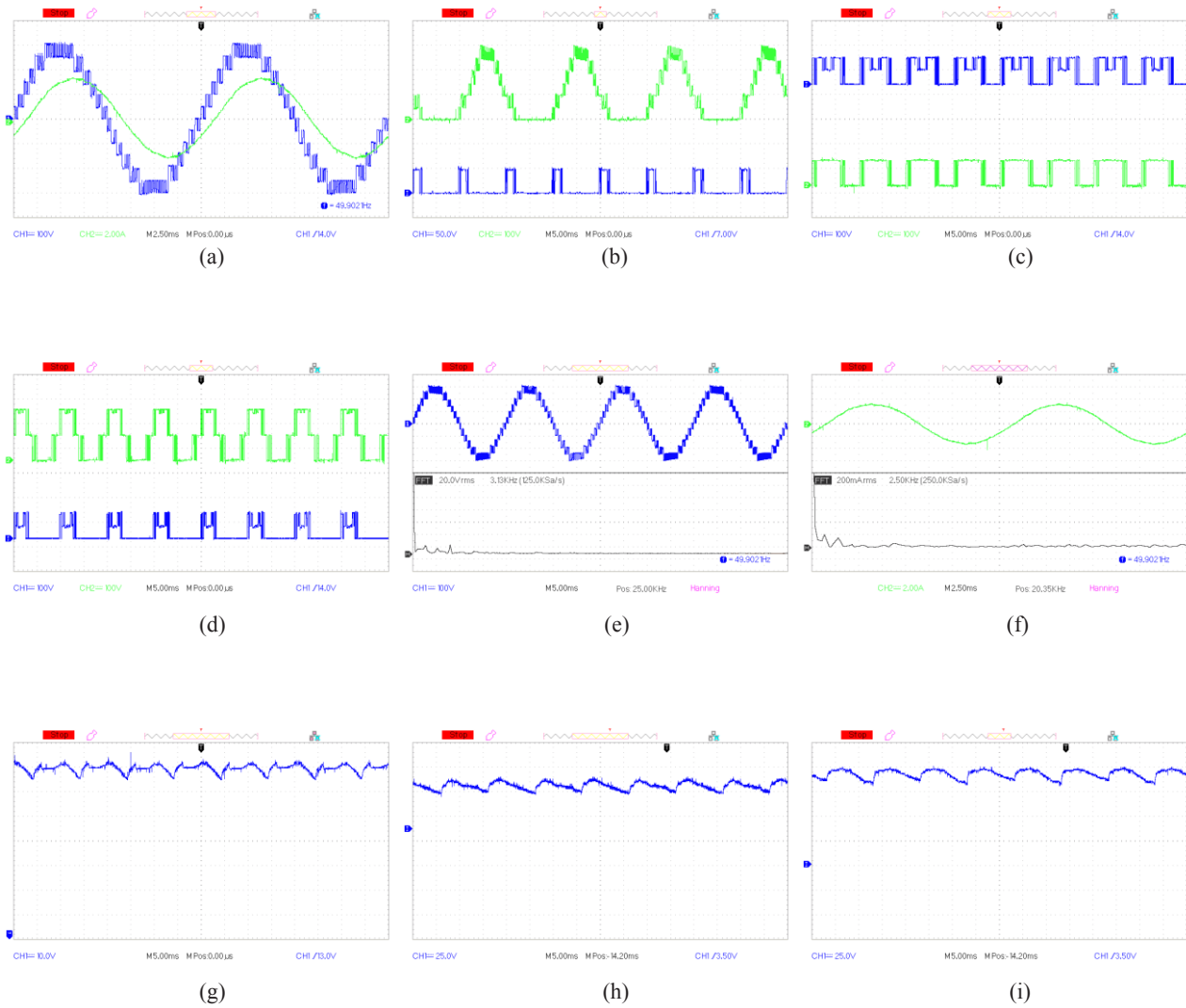


Fig. 18. The experimental waveforms: (a) for load voltage and load current, (b) for voltage stress across S1 and S12, (c) for voltage stress across S2 and S3, (d) for voltage stress across S5 and S6, (e) for harmonic spectrum of thirteen-Level load voltage, (f) for harmonic spectrum of load current, (g),(h), and (i) for capacitors voltage of C1, C2, and C3.

theoretical efficiency was calculated with detail. Meanwhile, a comparison of the proposed inverter with the existing similar inverters validates its merits. To assure the advantages and performance of the novel proposed 13-LFCI, it has been simulated and analyzed under different operation modes through MATLAB/ SIMULINK software and a 500 VA built set-up.

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