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A New Topology of Embedded Z-H Buck-Boost Converter

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ABSTRACT: In this paper, a new embedded Z-H (EZ-H) buck-boost converter is proposed. In this topology, two identical dc voltage sources are embedded in a LC network in a series connection with the inductors. The proposed converter eliminates the shoot-through (ST) switching state and there is no need for a front-end diode. Other advantages of the proposed topology are having capability of buck and boost operations in one structure; reaching the maximum gain in the duty cycle near 0.5; lowering ripples of voltage and current; and particularly reducing the voltage stress on the capacitors. In this paper, the voltage and current equations of all the components are extracted with considering all the operation modes. In addition, a suitable switching method is presented for the proposed converter to generate the desired output voltage. The ripple values of inductors and capacitors are calculated. Simulation results by the PSCAD/EMTDC software show accuracy and performance of the proposed .converter

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1- Introduction

The voltage source inverters operate only in buck mode, which makes them unsuitable for renewable energy applications. To increase the voltage magnitude, a dc-dc converter is used. In order to increase or decrease the output voltage, without an additional converter, an X-shaped LC network, namely Z-source inverter can be used [1-3]. The Z-source inverters are used in many applications such as adjustable speed drives [4-5], uninterruptable power supplies (UPS) [6-7], photovoltaics [8-10], wind turbine [11-12], etc.

The main features of Z-source inverters are a) the ST zero state makes the magnitude of output voltage lower or higher than the magnitude of a source voltage without any need to buck or boost converters or transformers; b) the LC network enhances the reliability. Adding two inductors and two capacitors to the voltage source inverter increases the size. In order to increase the power density of the system, the size of capacitors and inductors must be decreased, which can be done by modification in the Z-source inverter structure.

Over the recent years, several Z-source inverter structures with different capabilities have been proposed. Embedded Z-source (EZ-source) inverter and series Z-source inverter are two modified structures [13-16]. In the EZ-source inverter, the voltage of capacitor and input current are decreased due to the dc voltage source in series with the inductor. In series Z-source inverter, the voltages of two capacitors are decreased due to the dc voltage source in series with the bridge inverter. In the modified Z-source inverters, the size and cost of capacitors are decreased, which make the size of inductors smaller and therefore power density of the system is increased.

The diode (switch) before LC network (front-end diode) has some disadvantages, a) it makes the current waveform non-continuous, which causes inappropriate condition during non-shoot-through state; b) it prevents flowing reverse currents, which causes to be used in applications that do not require reverse flow of energy capability [1, 17].

In order to overcome the aforementioned problems, the Z-H converter was proposed in [17], which has one structure for buck conversion and another one for boost conversion. Buck and boost Z-H converters eliminate the front-end diode and shoot-through state.

The main disadvantage of this Z-H converter is that to increase or decrease the output voltage, two separate structures must be used [17, 18]. Another structure based on Z-H structure has been presented in [19] as a buck-boost Z-H converter, which has two capabilities of buck and boost conversion in one structure.

In this paper, in order to overcome the problems of the Z-H converter, using the concepts of Z-source inverter, Z-H converters, and an embedded voltage source, a new converter is proposed, which has buck and boost capabilities in one structure and particularly decreases the voltage stress across capacitors.

In order to evaluate the proposed structure, the equations of voltage, current waveforms, and voltage gain are obtained and the ripple values of inductors' and capacitors' voltage are given. A suitable switching method is presented. Also, the converter is simulated in PSCAD/EMTDC and results are presented.

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2- Proposed EZ-H Buck-Boost Converter

Fig. 1 shows the structure of the proposed EZ-H buck-boost converter. Like the Z-source inverter, this structure contains an LC impedance network and similar to the Z-H converter, this structure eliminates the front-end diode of the LC network. This structure differs from those of the Z-source inverter and the Z-H converter in terms of topology but resembles them in terms of operating principles. In the proposed topology, two dc input sources with values of $V_i/2$ are used in series with inductors of the LC network. The switches in Fig. 1 are of bidirectional types from voltage and current points of view. The inductors L_1 and L_2 filter the current drawn from the dc sources which resolves the need for additional filter [15].

In the conventional Z-source, the diode before the LC network creates an unfavorable operation mode during the non-ST state. In addition, it prevents the reverse current, which confines the use of this converter to the applications with no need to energy return to the input source [1, 17-18]. However, in the proposed converter, the front-end diode is eliminated.

The proposed converter can produce lower or higher voltage than the input voltage. Due to the existence of LC network, the reliability of the converter is increased. The proposed structure can be applied for dc-dc, dc-ac and ac-dc conversions without any change in its structure. Moreover, it eliminates ST switching state due to Z-source LC network.

In conventional Z-source inverters, the number of the switches is higher than the one in the proposed converter. Also, the conventional Z-source inverter has a front-end diode that adds to the losses of the inverter. Therefore, in the similar conditions, according to [19, Eq. 76], power loss in the conventional Z-source inverter is higher than the power loss in the proposed converter, and this shows the higher efficiency of the proposed converter in comparison with the conventional Z-source inverter.

The proposed converter consists of two operating zones. Over $D=[0,0.5)$, the converter operates in buck-boost mode and over $D=(0.5,1]$, it operates in boost mode. In Fig. 1, S_1 is turned on complementary with S_3 and S_2 is turned on complementary with S_4 (when S_1 and S_4 are on, S_2 and S_3 are off and vice versa). The duty cycle for S_2 and S_3 is defined as $D=T_0/T$ in which T_0 is the turn-on interval time of the switch in switching period of T. Fig. 2 shows the waveforms of control signals for the two operating zones, i.e. $D=[0,0.5)$ and $D=(0.5,1]$. In order to generate the switching signals, a triangular carrier wave (A_c) is compared to a constant reference signal (A_r). If the triangular carrier wave exceeds the reference signal, the switches S_1 and S_4 are turned on and S_2 and S_3 are turned off and vice versa. In the following, the different operating modes of the converter are investigated.

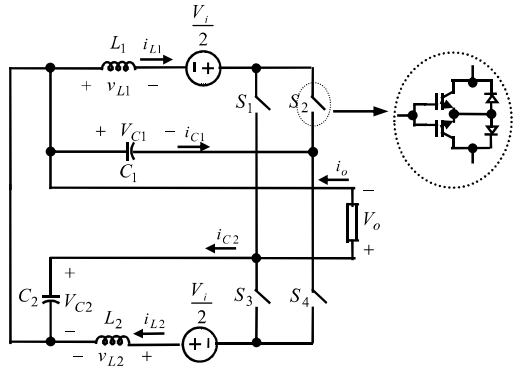


Fig. 1. Proposed EZ-H buck-boost converter

- *First Operating Mode (Time Interval T_0)*

Fig. 3(a) shows the equivalent circuit of the proposed converter for the first operating mode. The switches S_2 and S_3 are on and the switches S_1 and S_4 are off. In $D=[0,\ 0.5)$, the inductors L_1 and L_2 are charged by the capacitor C_1 and the voltage source $V_i/2$, and the capacitor C_2 and the voltage source $V_i/2$, respectively. In $D=(0.5,\ 1]$, the inductors L_1 and L_2 are discharged by the capacitor C_1 and the voltage source $V_i/2$; and by the capacitor C_2 and the voltage source $V_i/2$, respectively. Assuming that $L_1=L_2=L$ and $C_1=C_2=C$, we have:

$$V_{C1}=V_{C2}=V_C, \tag{1}$$

$$v_{L1}=v_{L2}=v_L, \tag{2}$$

where V_C and v_L are the voltage across capacitors and inductors, respectively.

For T_0 (Fig. 3(a)), the following equations can be written:

$$v_{L,T0}=0.5V_i+V_C \tag{3}$$

$$V_{o,T0}=V_C \tag{4}$$

where V_i and V_o are the input and output voltages of the converter, respectively.

- *Second Operating Mode (Time Interval T_1)*

Fig. 3(b) shows the equivalent circuit of the proposed converter for the second operating mode. The switches S_1 and S_4 are on and the switches S_2 and S_3 are off. In $D=[0,\ 0.5)$, the inductors L_1 and L_2 are discharged by the capacitor C_2 and the voltage source $V_i/2$; and by the capacitor C_1 and the voltage source $V_i/2$, respectively. In $D=(0.5,\ 1]$, the inductors L_1 and L_2 are charged by the capacitor C_2 and the voltage source $V_i/2$; and by the capacitor C_1 and voltage source $V_i/2$, respectively.

For T_1 (Fig. 3(b)), the following equations are obtained,

$$v_{L,T1}=0.5V_i-V_C, \tag{5}$$

$$V_{o,T1}=V_C. \tag{6}$$

According to (4) and (6), the values of output voltage are equal in T_0 and T_1.

2- 1- Extraction of Voltages' Equations and Voltage Gain

Considering the voltage balancing law, the average voltage of an inductor is zero. Thus, from (3) to (6), the average voltage across capacitors (V_C) and the average output voltage (V_o) in the both operating zones and the both time intervals T_0 and T_1 are given by

$$\begin{aligned} V_o=V_C&=\left(\frac{1}{1-2D}\right)\frac{V_i}{2}>0 \quad for \quad D=[0,\ 0.5)\\ &=\left(\frac{1}{1-2D}\right)\frac{V_i}{2}<0 \quad for \quad D=(0.5,\ 1]. \end{aligned} \tag{7}$$

Considering (7), the voltage gain (B) of the converter can be defined as:

$$B=\frac{V_o}{V_i}=\left(\frac{0.5}{1-2D}\right)$$

$$for \quad D=[0,\ 0.5)\ \&\ D=(0.5,\ 1]. \tag{8}$$

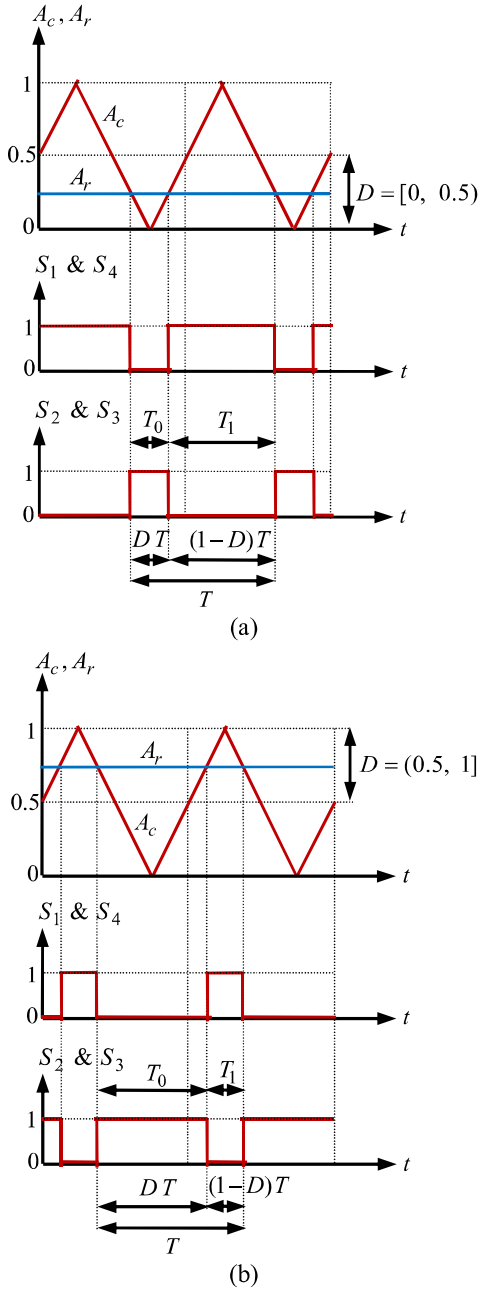


Fig. 2. Switching signals for two operating zones; (a) *D =[0,0.5)*; (b) *D = (0.5,1]* .

As Fig. 4(a) shows, in $D=[0,\ 0.5)$ the converter operates as buck where $0 \le D < 0.25$ and $0 \le B \le 1$ and as boost where $0.25 < D < 0.5$ and $1 \le B \le +\infty$. In $D=(0.5,\ 1]$, the converter operates as boost where $-\infty < B \le -1$. Fig. 4(b) compares the voltage stress across capacitors for the Z-H converter [17] and the proposed EZ-H converter. The output voltage is positive in the first operating zone and is negative in the second operating zone. Figs. 4(a) and 4(b) also show that in comparison with the Z-H converter, EZ-H converter has buck-boost characteristics in one structure.

2- 2- Extraction of Currents' Equations

For the time interval T_0 (Fig. 3.(a)), the following equations are obtained:

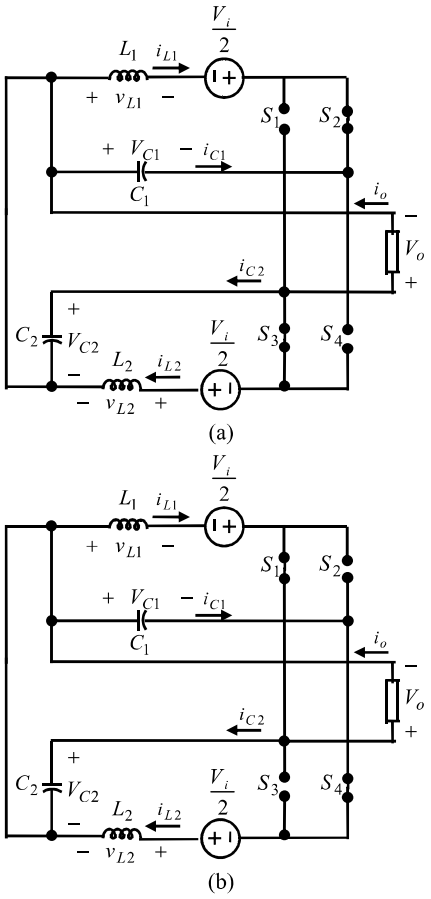


Fig. 3. The equivalent circuit of proposed EZ-H converter; (a) in time interval T_0; (b) in time interval T_1.

$$i_{C1,T0} = i_{o,T0} - i_{L1,T0}, \tag{9}$$

$$i_{C2,T0} = -i_{L2,T0}, \tag{10}$$

where i_C and i_L are the instantaneous currents through the capacitors and the inductors, respectively. Also, i_o is the output current of the converter.

For the time interval T_1 (Fig. 3(b)), the following equations are obtained:

$$i_{C1,T1} = i_{L2,T1}, \tag{11}$$

$$i_{C2,T1} = -i_{L2,T1}. \tag{12}$$

Assuming that the load is purely resistive, the instantaneous output current (i_o) and the average output current ($I_{o,av}$) in the both operating zones and the both time intervals can be given by:

$$i_o = i_{o,av} = \frac{V_o}{R_L} \tag{13}$$

Assuming that the initial current of the inductor at the beginning of the time interval T_0 is equal to I_1, the instantaneous current through the inductor (i_L) in the time interval T_0 can be given by:

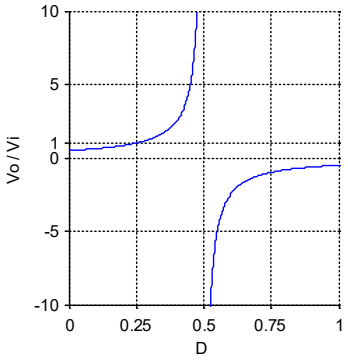
$$i_{L,T0} = \frac{0.5V_i + V_C}{L}t + I_1 \quad for \quad 0 \le t \le T_0 \tag{14}$$

In order for instantaneous current through the inductor in the time interval T_0 to be ascending in the first operating zone and descending in the second operating zone, the following

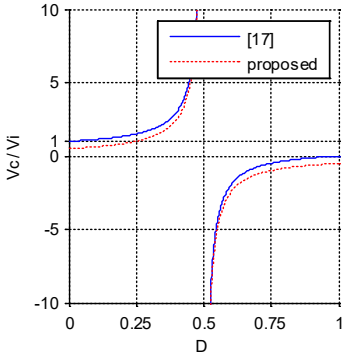
conditions must be satisfied:

$$\frac{di_{L,T0}}{dt} > 0 \quad \& \quad V_C > -0.5V_i \quad for \quad D = [0,\ 0.5), \tag{15}$$

$$\frac{di_{L,T0}}{dt} < 0 \quad \& \quad V_C < -0.5V_i \quad for \quad D = (0.5,\ 1]. \tag{16}$$



(a)



(b)

Fig. 4. (a) Variation of voltage gain versus duty cycle for the proposed converter; (b) Comparison of Z-H [17] and proposed EZ-H converters in terms of voltage stress across capacitors.

By considering $t = T_0 = DT$ in (14), the current through the inductor at the end of the time interval T_0, I_2, can be obtained as follows:

$$i_{L,T0}\big|_{t=T0=DT} = I_2 = \frac{0.5V_i + V_C}{L}T_0 + I_1 = \frac{0.5V_i + V_C}{L}DT + I_1. \tag{17}$$

If the initial current of the inductor at the beginning of the time interval T_1 is assumed to be I_2, the instantaneous current through the inductor in this time interval can be given by:

$$i_{L,T1} = \frac{0.5V_i - V_C}{L}t + I_2 \quad for \quad 0 \le t \le T_1. \tag{18}$$

In order for instantaneous current through the inductor in the time interval T_1 to be descending in the first operating zone and ascending in the second operating zone, the following conditions must be satisfied:

$$\frac{di_{L,T1}}{dt} < 0 \quad \& \quad (0.5V_i - V_C < 0 \ or \ 0.5V_i < V_C) \quad for \quad D = [0,\ 0.5), \tag{19}$$

$$\frac{di_{L,T1}}{dt} > 0 \quad \& \quad (0.5V_i - V_C > 0 \ or \ 0.5V_i > V_C) \quad for \quad D = (0.5,\ 1]. \tag{20}$$

Considering the inequalities (15), (16), (19), and (20), the conditions for controllable power transfer in the first and second operating zones are given as it follows,

$$V_C > -0.5V_i \quad \& \quad 0.5V_i < V_C \quad for \quad D = [0,\ 0.5), \tag{21}$$

$$V_C < -0.5V_i \quad \& \quad 0.5V_i > V_C \quad for \quad D = (0.5,\ 1]. \tag{22}$$

According to (21), in the first operating zone, the voltage across the capacitor must be positive and ±0.5 times more than the input voltage. Regarding (22), in the second operating zone, in order for the power to be transferred from the input voltage source to the output, the voltage across capacitor must be negative and the input voltage must be times as much as the capacitor voltage.

By letting $t = T_1 = (1-D)T$ in (18), the current through the inductor at the end of the time interval T_1, i.e. I_1, can be obtained as:

$$i_{L,T1}\big|_{t=T1=(1-D)T} = I_1 = \frac{0.5V_i - V_C}{L}T_1 + I_2 = \frac{0.5V_i - V_C}{L}(1-D)T + I_2. \tag{23}$$

Using (17) and (23), the average value of the current through each of the inductors in both the operating zones can be given by

$$I_{L,av} = \frac{1}{T}\int_0^T i_L\,dt = \frac{1}{2Lf}\Big[(0.5V_i + V_C)D^2 + (0.5V_i - V_C)(1-D)^2\Big] + DI_1 + (1-D)I_2, \tag{24}$$

where $f = 1/T$ denotes the switching frequency of the converter.

Considering (17), (23) and (7), the current ripples of the inductors can be obtained as:

$$\Delta I_{L1} = \Delta I_{L2} = |I_2 - I_1| = \frac{0.5V_i + V_C}{L}DT = \left|\frac{D(1-D)}{(1-2D)}\right|\frac{V_i}{Lf} \quad for \quad D = [0,\ 0.5)\ \&\ D = (0.5,\ 1]. \tag{25}$$

According to the current balance law on the capacitor C_1, the average current through the inductors L_1 and L_2, say $I_{L1,av}$ and $I_{L2,av}$ respectively, can be given by

$$I_{L1,av} = \left(\frac{1-D}{(1-2D)^2}\right)\frac{V_i}{2R_L} \quad for \quad D = [0,\ 0.5) \ \& \ D = (0.5,\ 1], \tag{26}$$

$$I_{L2,av} = \left(\frac{D}{(1-2D)^2}\right)\frac{V_i}{2R_L} \quad for \quad D = [0,\ 0.5) \ \& \ D = (0.5,\ 1]. \tag{27}$$

The average value of inductor current, say $I_{L,av}$, can be defined by

$$I_{L,av} = \frac{I_1 + I_2}{2}. \tag{28}$$

The following equation defines the current ripple of the inductor (ΔI_L),

$$\Delta I_L = I_2 - I_1. \tag{29}$$

Considering (28) and (29), the values of I_1 and I_2 can be calculated as it follows,

$$I_1 = \frac{2I_{L,av} - \Delta I_L}{2} \; for \; D = [0, 0.5) \; \& \; D = (0.5, 1], \tag{30}$$

$$I_2 = \frac{2I_{L,av} + \Delta I_L}{2} \; for \; D = [0, 0.5) \; \& \; D = (0.5, 1]. \tag{31}$$

The instantaneous currents through the capacitors C_1 and C_2 at the end of the time intervals T_0 and T_1, $I'_{2,V}$ and $I'_{1,P}$, can be given by:

$$I'_{2,C1} = I'_{2,C2} = I'_{2,V} = -I_{2,L1}, \tag{32}$$

$$I'_{1,C1} = I'_{1,C2} = I'_{1,P} = I_{1,L2}. \tag{33}$$

Considering (32) and (33), the voltage ripple across the capacitors, say ΔV_C, in both the operating zones can be calculated as it follows,

$$\Delta V_{C1} = \Delta V_{C2} = \Delta V_C = \left| \pm \frac{D(I_{L1,av})}{C f} \right|. \tag{34}$$

According to (1)-(34), Fig. 5 shows the voltage and the current waveforms of the proposed EZ-H converter in the first operating zone.

According to (26) and (27), it can be observed that the average currents flowing through the inductors of the proposed converter are not equal. It is due to the fact that the series connection of the inductor and the dc input source of the upper and the lower parts of the converter are not symmetrical. This causes different powers to be taken from the input sources. Therefore, this will harden the control of the input powers for achieving maximum power. However, this problem can be solved by changing the structure of the proposed circuit.

3- Designing Values of *L* and *C*

Ripples of capacitor voltage and inductor current affect the stability of the converters. To properly design the values of C_1 and C_2, the allowable voltage ripple $x_C\%$ may be used, which is defined as it follows [20],

$$x_{C1}\% = x_{C2}\% = x_C\% = \frac{\Delta V_C}{V_C}. \tag{35}$$

Considering (26) and by inserting the values of V_C and ΔV_C from (7) and (34) into (35), the rated value of C_1 and C_2 are calculated as it follows,

$$C_1 = C_2 = C = \frac{D(1-D)}{f \, R_L (1-2D) x_C\%} \tag{36}$$

To properly design the values of L_1 and L_2, the allowable current ripples $x_{L1}\%$ and $x_{L2}\%$ may be used, which are defined as it follows,

$$x_{L1}\% = \frac{\Delta I_{L1}}{I_{L1,av}}, \tag{37}$$

$$x_{L2}\% = \frac{\Delta I_{L2}}{I_{L2,av}}. \tag{38}$$

By inserting the values of ΔI_{L1} and $I_{L1,av}$, given by (25) and (26), into (37), and by replacing the values of ΔI_{L2} and $I_{L2,av}$ from (25) and (27) with (38), the rated values of L_1 and L_2 are calculated as it follows,

$$L_1 = \frac{2D(1-2D)R_L}{f \, x_{L1}\%}, \tag{39}$$

$$L_2 = \frac{2(1-D)(1-2D)R_L}{f \, x_{L2}\%}. \tag{40}$$

4- Imulation Results

In order to evaluate accurate operation of the proposed EZ-H converter, simulations are performed in PSCAD/EMTDC software. Table 1 gives the values of the parameters used in the simulations. Fig. 6 illustrates the simulation results in the first operating zone for the buck operation by assuming $B = 0.625$ and $D = 2.5$ and for the boost operation by assuming $B = 2.5$ and $D = 0.4$.

Table 1. The values of the parameters used in the simulations.

Switching frequency (f)	Output load (R_L)	The LC network		Input voltage source ($\frac{V_i}{2}$)
		$C_1 = C_2$	$L_1 = L_2$	
$50\,kHz$	100Ω	$25\,\mu F$	$1\,mH$	$24V$

4- 1- Calculating Values of Capacitors and Inductors

Based on the discussions given in Section 3, the values of capacitors and inductors can be obtained as it follows.

Assume that $D = 0.4$, $\Delta I_{L1} = \Delta I_{L2} = 1.15A$, $V_C = 120\,V$ and $\Delta V_{C1} = \Delta V_{C2} = 1.15\,V$. From (35), the allowable voltage ripple $x_C\%$ is given by:

$$x_{C1}\% = x_{C2}\% = \frac{\Delta V_C}{V_C} = \frac{1.15}{120} = 0.0095$$

From (36), the rated values of the capacitances C_1 and C_2 are

$$C_1 = C_2 = \frac{D(1-D)}{f \, R_L (1-2D) x_C\%} = 25\mu F$$

From (37) and (38), the allowable current ripples $x_{L1}\%$ and $x_{L2}\%$ are given by

$$x_{L1}\% = \frac{\Delta I_{L1}}{I_{L1,av}} = 0.32,$$

$$x_{L2}\% = \frac{\Delta I_{L2}}{I_{L2,av}} = 0.48.$$

From (39) and (40), the rated values of the inductances L_1 and L_2 are obtained from the following relations,

$$L_1 = \frac{2D(1-2D)R_L}{f \, x_{L1}\%} = 1mH,$$

$$L_2 = \frac{2(1-D)(1-2D)R_L}{f \, x_{L2}\%} = 1mH.$$

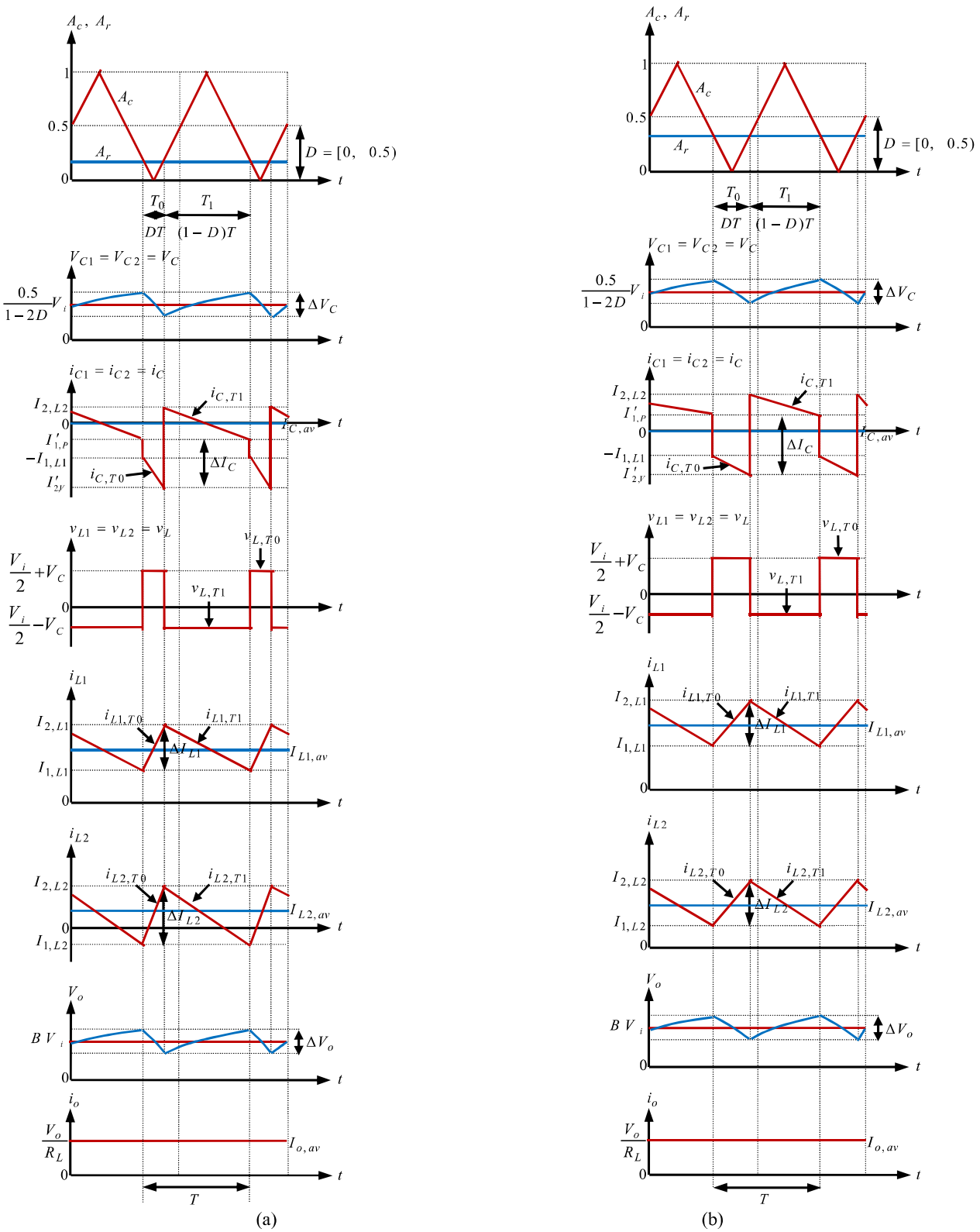
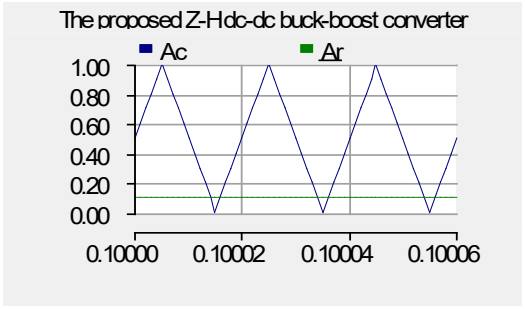
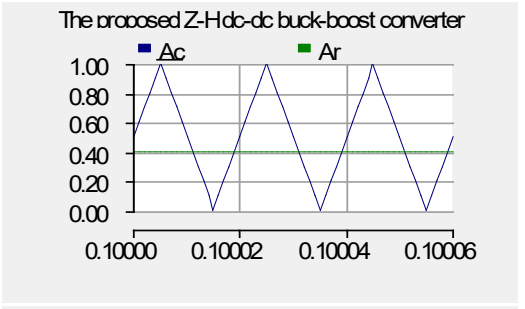


Fig. 5. Voltage and current waveforms of the proposed EZ-H converter in the first operating zone, where $D=[0,0.5)$; (a) buck; (b) boost.


The proposed Z-H dc-dc buck-boost converter
Ac
Ar
1.00
0.80
0.60
0.40
0.20
0.00
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
Ac
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1.00
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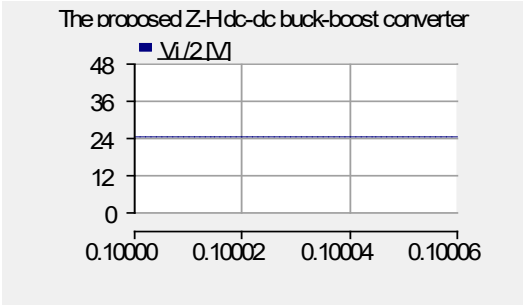
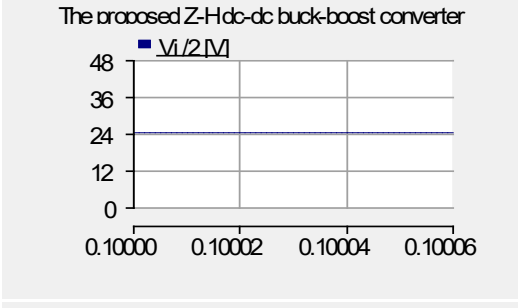

The proposed Z-H dc-dc buck-boost converter
Vi /2 [V]
48
36
24
12
0
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
Vi /2 [V]
48
36
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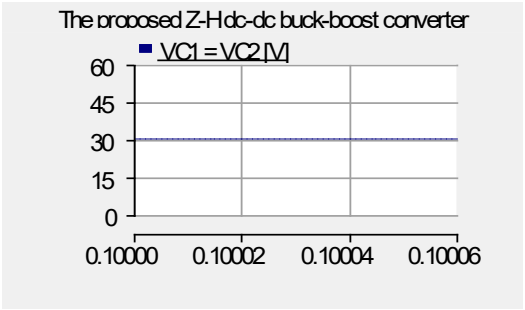
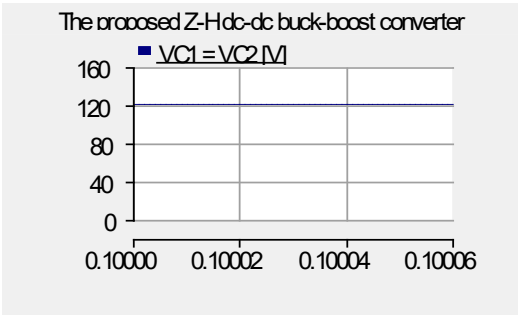
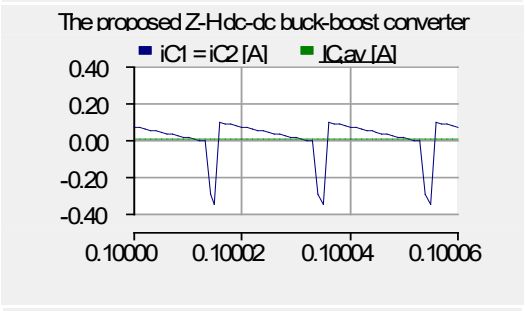
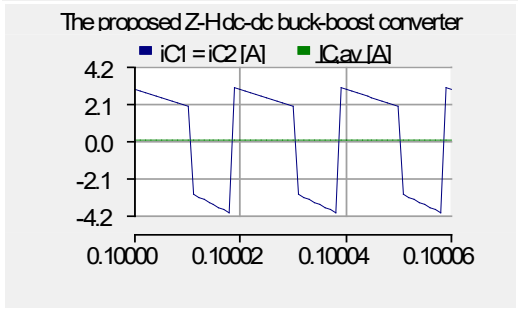
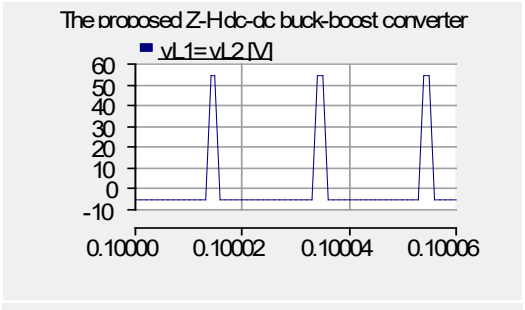
0.10004
0.10006

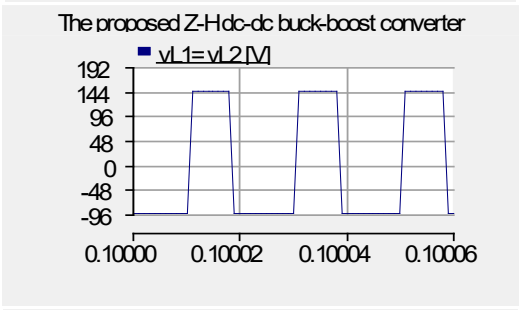

The proposed Z-H dc-dc buck-boost converter
VC1 = VC2 [V]
60
45
30
15
0
0.10000
0.10002
0.10004
0.10006

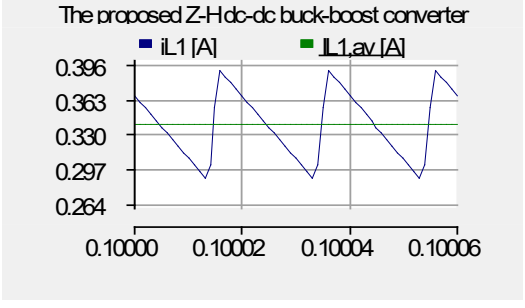

The proposed Z-H dc-dc buck-boost converter
VC1 = VC2 [V]
160
120
80
40
0
0.10000
0.10002
0.10004
0.10006

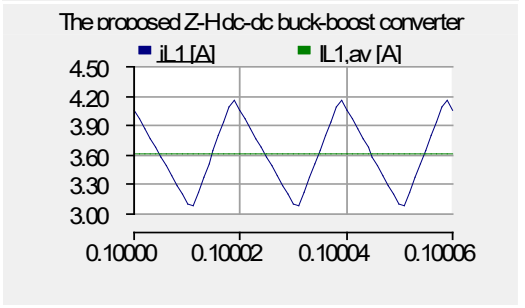

The proposed Z-H dc-dc buck-boost converter
iC1 = iC2 [A]
IC,av [A]
0.40
0.20
0.00
-0.20
-0.40
0.10000
0.10002
0.10004
0.10006

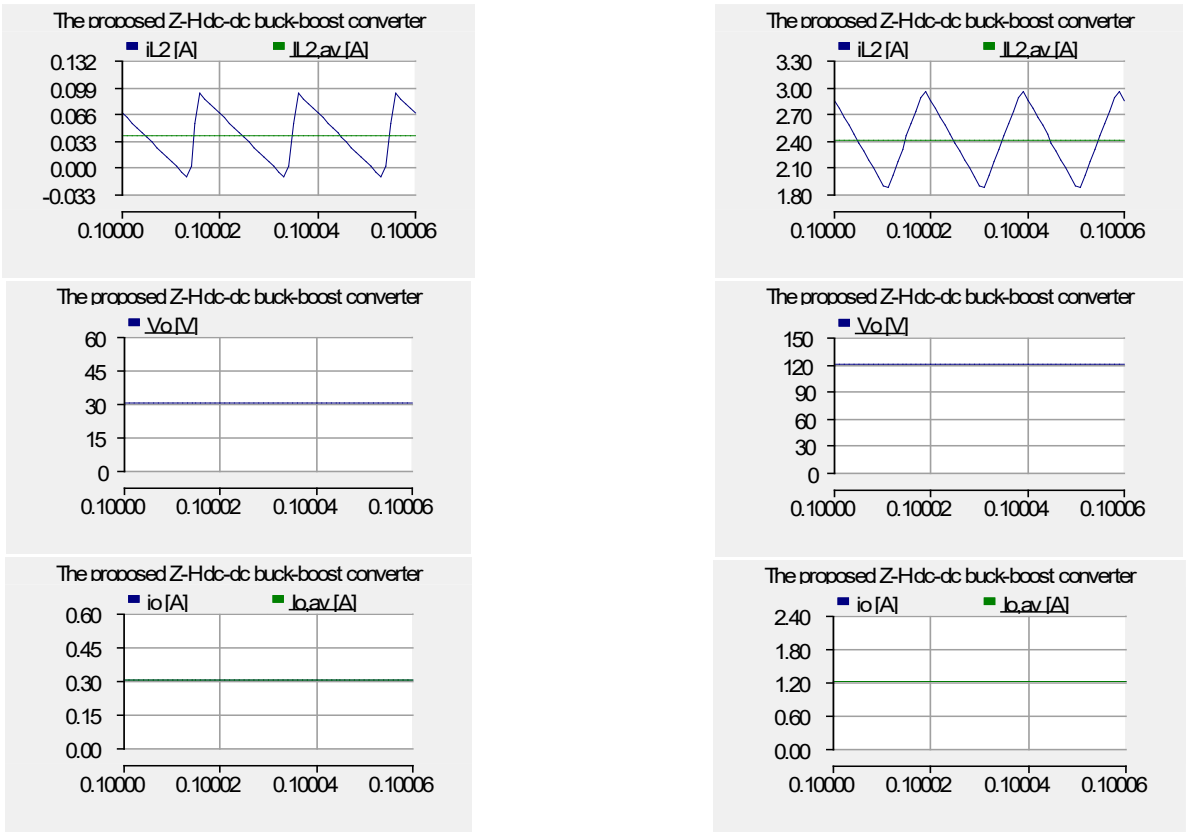

The proposed Z-H dc-dc buck-boost converter
iC1 = iC2 [A]
IC,av [A]
4.2
2.1
0.0
-2.1
-4.2
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
vL1= vL2 [V]
60
50
40
30
20
10
0
-10
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
vL1= vL2 [V]
192
144
96
48
0
-48
-96
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
iL1 [A]
IL1,av [A]
0.396
0.363
0.330
0.297
0.264
0.10000
0.10002
0.10004
0.10006


The proposed Z-H dc-dc buck-boost converter
iL1 [A]
IL1,av [A]
4.50
4.20
3.90
3.60
3.30
3.00
0.10000
0.10002
0.10004
0.10006



(a) (b)

Fig. 6. Simulation results of the proposed EZ-H buck-boost converter in the first operating zone (*D=[0,0.5)*); (a) buck mode for *B=0.625* and *D=0.1*; (b) boost mode for *B=2.5* and *D=0.4*.

4- 2- Calculation of Voltages and Currents Values

From (7) and (13), the output voltage and current of the converter in the time intervals T_0 and T_1 are $V_o = 120V$ and $i_o = 1.2A$, respectively. Considering (7), the average voltage across capacitors C_1 and C_2 in both the time intervals is $V_C = 120V$. From (3) and (5), the voltages across inductors L_1 and L_2 in the time intervals T_0 and T_1 are as $v_{L,T0} = 144V$ and $v_{L,T1} = -96V$, respectively. According to (25), the value of current ripples of inductors is $\Delta I_{L1} = \Delta I_{L2} = \Delta I_L = 1.15A$. From (26), (30) and (31), the average current through the inductor L_1 and the values of its current at the end of the time intervals T_0 and T_1 are $I_{L1,av} = 3.6A$, $I_{1,L1} = 3.02A$ and $I_{2,L1} = 4.17A$, respectively. Using (27), (30) and (31), the average current of the inductor L_2 and its current at the end of the time intervals T_0 and T_1 are $I_{L2,av} = 2.4A$, $I_{1,L2} = 1.82A$ and $I_{2,L2} = 2.97A$, respectively. Considering (32) and (33), the currents through the capacitors C_1 and C_2 at the end of the time intervals T_0 and T_1 are $I'_{2,C1} = I'_{2,C2} = -4.17A$ and $I'_{1,C1} = I'_{1,C2} = 1.82A$, respectively. From (34), the voltage ripples of the capacitors are $\Delta V_{C1} = \Delta V_{C2} = 1.15V$.

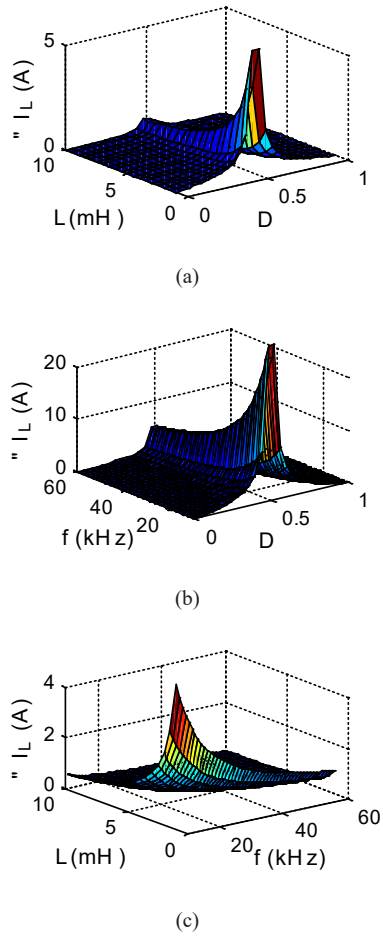
The results obtained from the simulations as in Fig. 6(b), confirm the accuracy of the theoretical calculations and correspond to the waveforms illustrated in Fig. 5(b). The above calculations are for the boost operation and in the same way can be repeated for the buck operation.

4- 3- Variations Analysis of the Current and Voltage Ripples

In order to show the variations of the inductor current ripple, capacitor voltage ripple, duty cycle, frequency, inductance and capacitance with respect to each other, Figs. 7 and 8 are given.

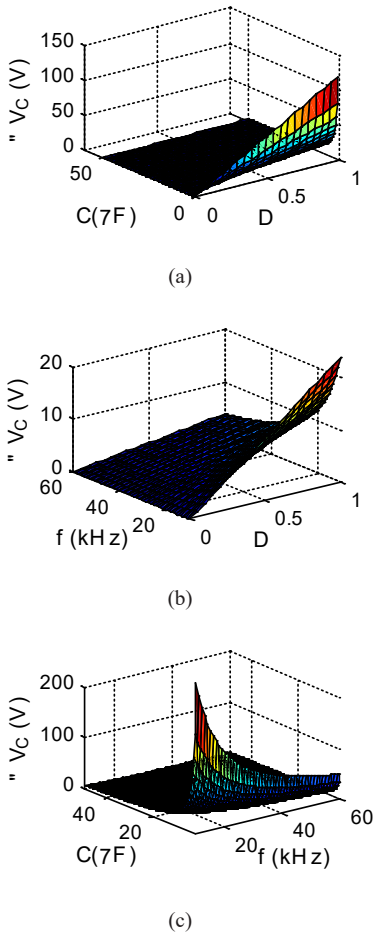
Fig. 7(a) shows the variations of the current ripple of the inductor versus the inductance and the duty cycle for specific values of the input voltage and the frequency. As the figure shows, the current ripple of the inductor increases by approaching the duty cycle $D = 0.5$ from both ends of the duty cycle. In addition, it is observed that for a specified duty cycle, the value of the current ripple of the inductor decreases as the value of the inductance increases. Fig. 7(b) shows the variations of the current ripple of inductor versus the frequency and the duty cycle for specific values of the input voltage and the inductance. As the figure shows, the current ripple of the inductor increases by approaching the duty cycle $D = 0.5$ from both ends of the duty cycle. In addition, it is observed that for a specified duty cycle, the value of the current ripple of the inductor decreases as the value of the frequency increases. Fig. 7(c) shows the variations of the current ripple of inductor versus the frequency and the inductance for specific values of the input voltage and the duty cycle $D = 0.6$. As can be seen, the value of the current ripple of inductor increases by decreasing the values of both the frequency and the inductance.

Fig. 8(a) shows the variations of the voltage ripple of the



(a) (b) (c)

Fig. 7. Variations of the inductor current ripple versus (a) duty cycle and the inductance; (b) duty cycle and the frequency and (c) frequency and the inductance



(a) (b) (c)

Fig. 8. Variations of the capacitor voltage ripple versus (a) duty cycle and the capacitance; (b) duty cycle and the frequency and (c) frequency and the capacitance

capacitor versus the capacitance and the duty cycle for certain values of the current ripple of the capacitor and the frequency. As the figure shows, the voltage ripple of the capacitor increases by increasing the duty cycle and decreasing the capacitance. Fig. 8(b) shows the variations of the voltage ripple of the capacitor versus the frequency and the duty cycle for certain values of the current ripple of the capacitor and the capacitance. As the figure shows, the voltage ripple of the capacitor increases by increasing the duty cycle and decreasing the frequency. Fig. 8(c) shows the variations of the voltage ripple of the capacitor versus the capacitance and the frequency for certain values of the current ripple of the capacitor and the duty cycle $D = 0.5$. As the figure shows, the voltage ripple of the capacitor increases by decreasing the values of the frequency and the capacitance.

From Figs. 7 and 8, it can be observed that the more the values of the frequency, the capacitance and the inductance, the less the current and the voltage ripples.

5- Conclusion

In this paper, a new Z-H buck-boost converter with embedded input voltage sources was proposed. In comparison with the Z-H conventional converter, the proposed converter reduces the voltage stress across capacitors. Elimination of ST switching state, no need to additional filtering and the front-end diode, buck-boost capability in one structure, achieving maximum voltage gain by duty cycle near 0.5, and lower ripples of voltage and current waveforms are the advantages of the proposed topology. The operating principles of the proposed converter were discussed and equations of voltage and current of all the elements of the proposed converter were obtained. Also, the optimum values of the inductors and the capacitors were given. The results obtained from the theoretical calculations and simulations in PSCAD/EMTDC showed the performance and effectiveness of the proposed converter.

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