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Design and implementation of a Single-Input Dual-Output Converter with Independent Control of Output Voltages

Zeynab Saeidi Taheri[1], Siroos Hemmati*[2], Vahid Abbasi[3]

[1]M.Sc., Department of Electrical Engineering, Kermanshah University of Technology.

[2]Associate Professor, Department of Electrical Engineering, Kermanshah University of Technology.

[3]Associate Professor, Department of Electrical Engineering, Kermanshah University of Technology.

***Corresponding author**: s.hemmati@kut.ac.ir

Abstract: This paper introduces a non-isolated single-input dual-output (SIDO) multiport DC-DC converter with applications in renewable energy systems, electric vehicles, uninterruptible power supplies, battery chargers, and personal computers. The proposed SIDO converter consists of two independent outputs**,** regulated at 110 V (as a boost stage) and 12 V (as a buck stage), respectively. Key features include an optimal 12-component count, continuous input currents, a common-ground architecture, and independent controllability of output voltages. Furthermore, the converter achieves the desired voltage gain, low voltage stress on diodes and switches, and a high efficiency of approximately 93.1%. The system is designed for a 245.77 W total power rating, providing 132.5 W for the boost stage and 113.3 W for the buck stage. The proposed topology is tested in the laboratory, and the experimental results verify the proper performance of the converter.

Keywords: Multi-port converter, Single-input multiple-output, Voltage stress, Common ground, DC-DC converter

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1. Introduction

The growing demand for electrical energy, coupled with serious environmental challenges such as global warming and pollution caused by fossil fuels, has driven scientific communities towards using renewable energy sources [1]. Among these, photovoltaic systems have become one of the main pillars of modern microgrids due to their high reliability and low operation costs. However, the intermittent nature of power generation in these sources and the need for different voltage levels in consumer loads, such as sensitive loads in electric vehicles or nano grids, has introduced new challenges in the design of power electronic converters [2]. Generally, the voltage level of renewable sources is low, and therefore, step-up converters must be used to increase the voltage of these sources [3]. Traditionally, supplying different voltages from a single source required the use of several separate converters connected to a common bus. This approach, due to the multiple stages of energy conversion, not only increases the system's volume and final cost but also reduces overall efficiency because of cumulative losses in passive and active elements [4]. To address these shortcomings, multi-port converters were introduced, which, by integrating ports into a single structure, enable centralized power management and improved power density. The structures of multi-port converters are generally divided into three categories: single-input single-output [3], multi-input single-output [5], and single-input multiple-output converters. Among these structures, non-isolated single-input multiple-output (SIMO) converters are highly popular in automotive and uninterruptible power supply (UPS) applications due to their common ground feature and elimination of bulky transformers [6].

Various structures have been investigated in the literature. [7] introduces a single-input dual-output converter based on the interleaved buck converter. Although this converter has two outputs, both of them are step-down, and the output voltages are not independently controlled. Furthermore, the input current in this topology is discontinuous due to the switching operation, which largely limits its direct connection to renewable sources and the precise implementation of maximum power point tracking (MPPT) algorithms. In another study [8], the presented topology provides both step-down and step-up capabilities in three different operating modes; however, this flexibility comes at the cost of an increased number of elements. Also, control limitations exist, making independent control of the outputs impossible.

The challenge of lacking a common ground is also unsolved in many designs. The proposed design in [9] is a converter with two step-down outputs for use in electric vehicles, where the presence of two switches makes the control of the outputs dependent. In this design, the number of elements is relatively high, and the absence of a common ground between the input and outputs increases the cost and complexity of using isolated drivers and sensors, leading to electromagnetic interference and noise in the system. This not only disrupts the stability of control loops but also severely reduces the overall system reliability. The modular single-input multi-output converter introduced in [10] can be generalized to have N outputs. However, it faces the challenges of a high number of component and the purely step-down nature of the outputs. In this design as well, the lack of a common ground and having high current ripple leads to intensified thermal losses in passive elements and power switches, significantly reducing overall efficiency. These severe fluctuations cause energy waste in photovoltaic systems and accelerate the degradation process and reduce the lifespan of batteries in battery-powered systems.

The coupled inductors have been used as a solution to increase voltage gain in various studies. In [11], a converter based on a coupled inductor, featuring soft switching and generalization to N step-up outputs is introduced, but the parallel configuration of the outputs prevents their independent control. In [12], the authors propose a single-input dual-output three-level topology for medium and high voltage levels, comprising both step-up and step-down outputs. Although the use of multilevel circuits reduces voltage stress on switches, it significantly increases the number of components. Also, the lack of a common ground due to the input diode is a major drawback. The converter in [13] is presented for electric vehicles, consisting of three structures - simple buck, quasi-boost, and buck with a modified switch. While it enables independent control of each output, the high number of components substantially increases the final manufacturing cost.

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In more detailed analyses, [14] introduces a converter where the control of the step-down outputs is dependent due to the coupled inductor, requiring a complex decoupling process, which leads to reduced dynamic response and increased sensitivity to parameter variations. In [15], a topology with two step-up outputs is presented that utilizes the switched-capacitor technique. Although this technique allows for the elimination of bulky magnetic elements, it faces the challenge of severe inrush currents during capacitor charging, increasing the stress on switches and reducing the component lifespan. In [16], a design with 14 components is presented that provides independent control of step-up outputs. However, lacking step-down output limits its application.

In the area of power quality improvement, the design introduced in [17], based on a buck converter, attempts to reduce output voltage ripple by adding a capacitor-inductor network. In this design, however, the outputs are not independent, it suffers from inrush current as well as significant losses in the coupled inductor. In [18], a coupled inductor is used to increase the voltage level in hybrid sources, which, despite enabling independent control, involves very high mathematical complexity and controller design. Finally, in [19], the authors present a converter based on the Luo topology, designed by integrating a super-lift Luo converter, a flyback structure, and the coupled inductor concept. In this advanced structure, both outputs operate in step-up mode, but due to the magnetic coupling nature of the coupled inductor, the control of the outputs are not independent, leaving a fundamental challenge in the output ports power managing.

Considering the mentioned limitations, this paper introduces a single-input dual-output (SIDO) converter capable of simultaneously generating two voltage levels: step-down (Buck) and step-up (Boost). The main advantages of this design are the elimination of control interference between the output ports, meaning that load variation in one port does not disrupt voltage stability in the other port. This feature, along with the benefits of having a common ground and continuous input current, makes the proposed converter an ideal choice for renewable energy applications. In the following sections, after theoretical analysis and circuit modeling of the proposed converter, its performance will be validated through simulations and experimental tests.

2. Proposed converter and performance evaluation in different modes

The proposed topology shown in Fig. 1 is a non-isolated single-input/dual-output structure consisting of 12 main elements including two active power switches S_1 and S_2, two inductors L_1 and L_2, four capacitors C_1, C_2, C_a and C_b, and four diodes D_1, D_2, D_3 and D_4. In the proposed circuit, the input port and both output ports have a common ground; a unique feature that eliminates the need for isolated drivers and improves the electromagnetic compatibility of the system. Unlike many conventional structures, in this converter, the input current is continuous and the outputs are topologically decoupled (isolated) from each other and the input source. From a control perspective, this design provides independent voltage regulation and simultaneously has boost and buck features in its ports. Also, it has to be mentioned that the bidirectional capability in this converter is a potential extension for the second output port (simulation only), not a proven hardware feature, which can allow for charge and discharge management in energy storage applications.

The operational structure of the proposed converter is defined based on three main operation modes. In the first mode, both output ports a and b are simultaneously in the active state and are responsible for supplying the loads. The second and third modes are assigned to the operation of output port a and b, respectively. In the following, the operation principle and circuit analysis in each of these three modes are examined in detail.

According to this configuration, the input voltage source and the loads connected to the first and second ports have a common reference point or ground. The placement of the inductor L_1 at the input part of the circuit ensures the continuity of the input current. Also, the switches S_1 and S_2, as control degrees of freedom, are responsible for independently adjusting the voltage at the output ports V_{o1} and V_{o2}. In the proposed structure, the capacitors C_1 and C_2 play a key role in transferring energy and achieving the desired voltage gain.

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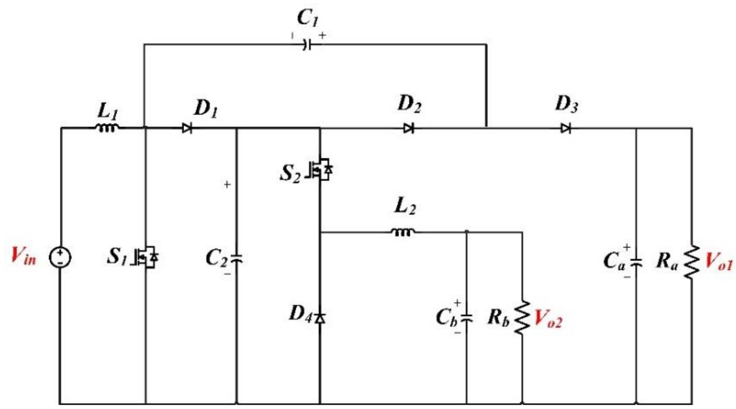

Fig. (1): Power circuit schematic of the proposed converter

2.1 mode I: both ports in operation

In this operating mode, the converter is controlled so that both output ports a and b are loaded simultaneously and provide the demanded power. One of the unique features of the proposed topology in this mode is the ability to achieve a boost voltage gain at one port and a buck-boost at the other port simultaneously. The current and voltage waveforms of the elements related to this mode are plotted in Fig. 2(a).

Analyzing the converter performance in a steady-state cycle requires examining three separate switching states as described below.

time interval (I) (t0-t1): In this interval, the switch S_1 is in the on state and the diodes D_2 and D_4 are also conducting. In contrast, the switch S_2 and the diodes D_1 and D_3 are in the off state. The equivalent circuit of the converter in this time interval is shown in Fig. (2)(b), showing the energy transfer paths and the charging and discharging of the energy storage elements.

time interval (II) (t1-t2): In the second state of the switching cycle, the state of the switches and diodes is changed so that the switch S_1 along with the diodes D_2 and D_4 are in the off state. In contrast, the switch S_2 and the diodes D_1 and D_3 start conducting. The equivalent circuit of this time interval, which shows the new power transfer paths and energy changes in the passive elements, is presented in Fig. (2)(c).

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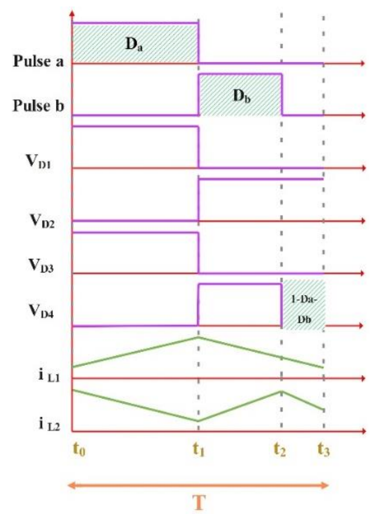
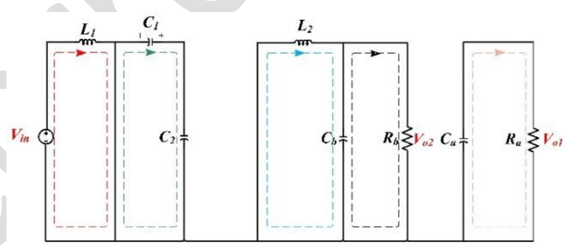
time interval (III) (t2-t3): In the last state of the switching cycle, both power switches S_1 and S_2 and diode D_2 are in the off state. In this condition, diodes D_1, D_3 and D_4 enter the conducting state and provide the necessary paths for transferring and discharging the energy of the magnetic elements to the outputs. The equivalent circuit corresponding to this time period, which shows how the current is distributed in this stage, is shown in Fig. (2)(d).



(a)



(b)

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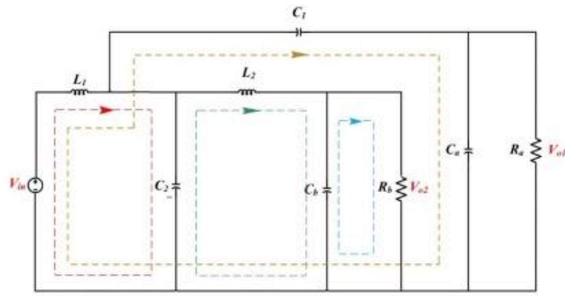
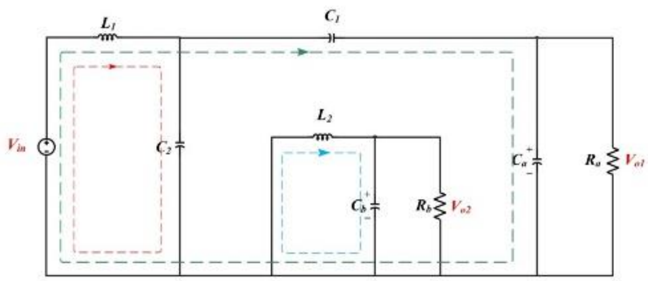


(c)



(d)

Fig. (2): (a) Key voltage and current waveforms of the elements in the first operational mode; (b) Equivalent circuit during the first interval; (c) Equivalent circuit during the second interval; (d) Equivalent circuit during the third interval

2.2 mode II: boost port operation

In this operating mode, the converter produces boosted voltage only at the first output (a); as a result, the step-down output port is inactive in this mode. In this mode, the switching signal is applied only to the power switch S_1 and, since the second switch is not activated, part of the circuit is effectively removed from the power transfer cycle. The key waveforms related to the voltage and current of the elements in this operating mode are depicted in Fig. (3)(a).

In analyzing the performance of the converter in this mode, there is a key important point: the first active interval does not start exactly from the switching time origin, i.e., the moment t_0. According to the adopted control strategy, in the time interval between the moment t_0 and t1, no command signal is applied to the

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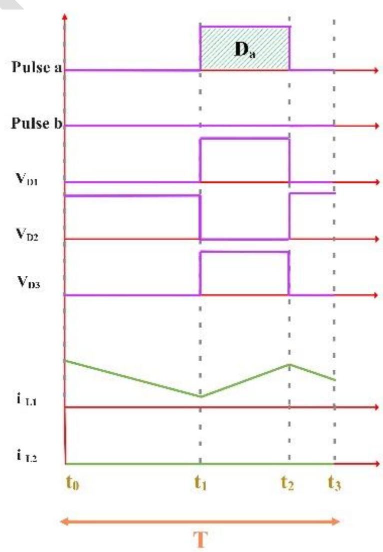
power switches; therefore, the circuit is in a waiting state or inactive phase in this interval. The main process of energy transfer starts from the moment t1 with the arrival of the first control pulse and continues until the moment t_2.

time interval (I) (t_1-t_2): By applying an excitation signal to the switch S_1, diodes D_1 and D_3 go to the cut-off state and diode D_2 starts conducting. The equivalent circuit of this time interval, which represents the energy transfer paths, is shown in Fig. (3)(b). In this state, the input inductor L_1 and the interface capacitor C_1 are storing energy (charging) and the voltages of capacitors C_1 and C_2 are equal to each other. Also, in this interval, the first output is powered by capacitor C_a.

time interval (II) (t_2-t_3): The switching state is changed and the switch S_1 along with the diode D_2 go to the OFF state. In contrast, the diodes D_1 and D_3 start conducting. The topology of the circuit at this stage is shown in Fig. (3)(d). In this state, by discharging the stored magnetic energy, the inductor recharges the capacitor C_2 (which was discharged in the previous stage). In other words, the inductor at this stage is simultaneously responsible for supplying the energy required by the first output load and managing the charging process of the capacitor C_2. A simplified schematic of the circuit at this stage is presented in Fig. (3)(d).



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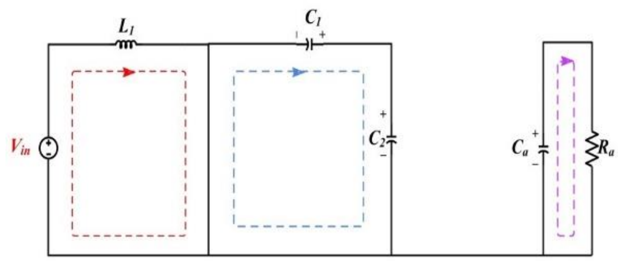
(a)



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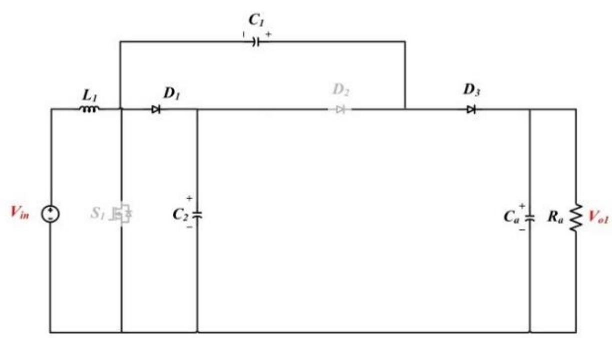
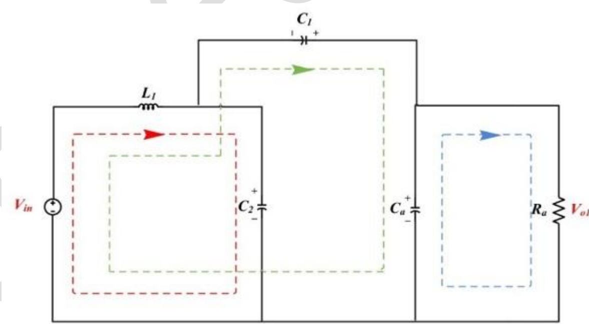


(c)



(d)

Fig. (3): (a) Key voltage and current waveforms of the elements in the second operational mode; (b) Equivalent circuit during the first interval; (c) Equivalent circuit during the second interval; (d) Simplified equivalent circuit during the second interval

2-3 mode III: second port operation

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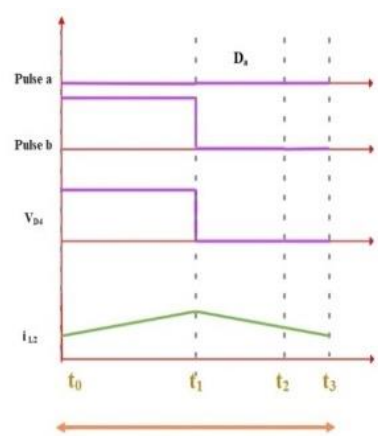
The last operation mode defined for this topology is the mode in which the converter is exclusively responsible for supplying power to the second output port (b). In this mode, the power switch S1 is in a permanently off state and does not receive excitation signal. In order to completely isolate the first output port (V_a) an isolation mechanism or hypothetical relay is considered after the diode D_3, which is responsible for removing the first load. In this configuration, the voltage regulation process is carried out only by switch S_2. Behavioral analysis of the circuit shows that when the switch S_2 is turned on, the diode D_4 is reverse biased, making the inductor L_2 to store energy. Conversely, when the switch S_2 is turned off, the diode D_4 is forward bias and, as a freewheeling diode, provides the necessary path for the energy discharge of the inductor L_2 towards the output load.

time interval (I): In the first state of this mode, switch S_2 starts conducting and the energy transfer path to the second output port is established. An important point in this situation is the role of the input passive elements. Since in this operating mode the switch S_1 is in a permanently off state, the inductor L_1 and the intermediate capacitor C_2 are removed from the active switching cycle and a second-order low-pass filter (LC Filter) is formed at the input.

time interval (II): In this period, the command signal to S_2 is also interrupted, the diode D_4 is placed in the conducting state, and the equivalent circuit is as shown in Fig. 4(c).



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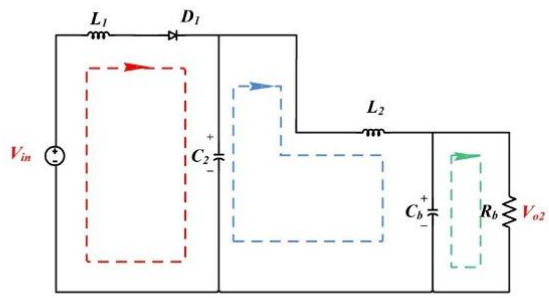
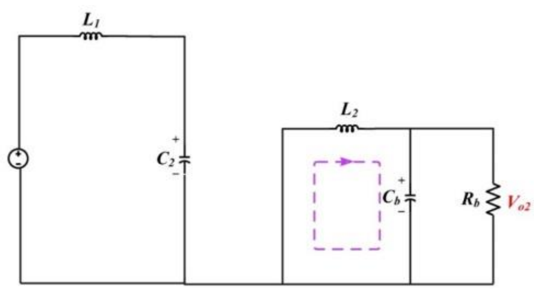
(a)



(b)



(c)

Fig. (4): (a) Key voltage and current waveforms of the elements in the third operational mode; (b) Equivalent circuit during the first interval; (c) Equivalent circuit during the second interval

3. Converter analysis in the first mode

According to Fig. 2(c) for the first interval, we have:

$$V_{in} = V_{L1} \quad (1)$$
$$V_{C1} = V_{C2} \quad (2)$$
$$V_{L2} = -V_{Cb} \quad (3)$$
$$V_{Cb} = V_b \quad (4)$$
$$V_{L2} = -V_b \quad (5)$$

Also for the second interval we have:

$$V_{L1} = V_{in} - V_{c2} \quad (6)$$

$$V_{L1} = V_{in} + V_{c1} - V_{o1} \quad (7)$$

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$$V_{L2} = V_{c2} - V_{o2} \tag{8}$$

Finally for the third interval we have:

$$V_{L1} = V_{in} - V_{c2} \tag{9}$$
$$V_{L1} = V_{in} + V_{c1} - V_a \tag{10}$$
$$V_{L2} = -V_b \tag{11}$$

Using the volt-second balance principle, for the first inductor we have:

$$\mathrm{D}_a \mathrm{VL}_1 + \mathrm{D}_b \mathrm{VL}_1 + (1 - \mathrm{D}_a - \mathrm{D}_b)\mathrm{VL}_1 = 0 \tag{12}$$

According to formulas (1), (6), and (9) we have:

$$\mathrm{D_a}(\mathrm{V_{in}}) + \mathrm{D_b}(\mathrm{V_{in}} - \mathrm{V_{C2}}) + (1 - \mathrm{D_a} - \mathrm{D_b})(\mathrm{V_{in}} - \mathrm{V_{C2}}) = 0 \tag{13}$$
$$\mathrm{V_{C2}} = \frac{\mathrm{V_{in}}}{1 - \mathrm{D_a}} \tag{14}$$

In the outputs, due to being in parallel, we have:

$$V_{o1} = V_a \tag{15}$$
$$V_{o2} = V_b \tag{16}$$

Again, by substituting the values of V_{L1} from relations (1), (7), and (10), we have:

$$V_{in} + V_{c1}(1 - D_a) = V_a(1 - D_a) \tag{17}$$

Now, we substitute relation (14) into (17) to obtain the voltage gain of the first output.

$$V_{o1} = V_a = \frac{2V_{in}}{(1 - D_a)} \tag{18}$$

Using the volt-second balance principle for the second inductor, we have:

$$D_a V_{L_2} + D_b V_{L_2} + (1 - D_a - D_b)V_{L_2} = 0 \tag{19}$$

Using relations (5), (8), (11), and (16), we have:

$$V_b = D_b V_{c2} \tag{20}$$

Also, by substituting (14) into (20), we obtain the following relation:

$$V_b = D_b \frac{V_{in}}{1 - D_a} \tag{21}$$

Therefore, the gain of the second output is obtained as follows:

$$V_{o2} = V_b = \frac{\mathrm{V_{in}}}{1 - \mathrm{D_a}} D_b \tag{22}$$

4. Components Design Guidelines

The design calculations for the proposed converter are done for $V_{in} = 24$ V, $P_o = 245$ W, $V_{o1} = 110$ V, $V_{o2} = 12$ V, $R_1 = 93$, $R_2 = 1.25$, $d_a = 0.56$, $d_b = 0.21$, and $f = 50$ kHz. The suggested converter's design enables it to function effectively at power levels that are both higher and lower than its nominal power. In addition, nominal conditions are used for the calculations, and the worst conditions are noticed for selecting the inductors, capacitors, and semiconductor devices.

A. Calculation of the inductances for the inductors

The inductors are designed based on the minimum inductance requirement, $L_{\min}$, to ensure continuous conduction mode (CCM) operation across the entire desired operating range. To guarantee that the converter consistently operates in CCM under the worst conditions, the maximum values of the minimum inductances ($L_{1-\min}$ and $L_{2-\min}$) are considered. To calculate $L_{1-\min}$ and $L_{2-\min}$, equations [23] and [24] should be used.

$$L_{1-min} = \frac{D_a(1-D_a)^2 R_1 R_2}{2f(4R_2 + D_b^2 R_1)} \tag{23}$$

$$L_2 \geq \frac{(1-D_b)R_2}{2f} \tag{24}$$

Based on (23), the analytical evaluation of $L_{1-\min}$ shows that the worst condition requiring the maximum inductance occurs at $d_a \cong 0.33$ (when $d_b = 0.4$), which concludes a maximum value of 50 μH. Similarly, from (24), $L_{2-\min}$ is independent of d_a and exhibits a negative linear dependency on d_b; thus, its worst condition demanding the maximum value occurs at the minimum operating duty cycle of d_b, which results in 70 μH. In both relations, operating at a lower output power (higher load resistance) increases the minimum required inductance boundary. To ensure continuous current under these worst conditions, the inductors for the prototype were selected to be greater than these calculated boundaries.

B. Design of the capacitors

Subsequently, the design guidelines for the capacitors are presented, focusing primarily on limiting the voltage ripple. The required capacitance values are then determined based on the converter parameters evaluated under the worst-case operating conditions.

$$I_{C1-on} = \frac{I_{O1}(1-D_b)}{D_b(1-D_a)} = C_1 \frac{d_{Vc1}}{d_t} \rightarrow C_1 \geq \frac{D_a \cdot V_{O1}(1-D_b)}{\Delta V_{C1} \cdot f_s \cdot R_1 \cdot D_b(1-D_a)} \tag{25}$$

$$I_{C2-on} = \frac{I_{O1}(1-D_b)}{D_b(1-D_a)} = C_2 \frac{d_{Vc2}}{d_t} \rightarrow C_2 \geq \frac{D_a \cdot V_{O1}(1-D_b)}{\Delta V_{C1} \cdot f_s \cdot R_1 \cdot D_b(1-D_a)} \tag{26}$$

$$I_{Ca-on} = I_O = C_a \frac{d_{Vca}}{d_t} \rightarrow C_a \geq \frac{D_a \cdot V_{O1}}{\Delta V_{Ca} \cdot f_s \cdot R_1} \tag{27}$$

$$I_{Cb-on} = C_b \frac{d_{Vcb}}{d_t} \rightarrow C_b \geq \frac{(1-D_b)V_{O2}}{8. L_2 . \Delta V_{Cb} \cdot {f_s}^2} \tag{28}$$

Considering the design parameters and limiting the voltage ripple, the minimum capacitance values are calculated using equations (25) to (28). The analytical results yield $C_1 \geq 280$ μF, $C_2 \geq 280$ μF, $C_a \geq 41$ μF and $C_b \geq 45$ μF. Due to practical component availability, capacitors with larger values were selected for the experimental prototype, which also offer the advantage of lower equivalent series resistance (ESR).

C. Semiconductor Selection

Semiconductor devices are selected based on the peak stress formulations compiled in Table (1), which are characterized under the worst-case scenario represented by Mode 1. To incorporate an adequate de-rating factor and safeguard the converter against overvoltage conditions, the breakdown voltage ratings of the chosen components are specified to be at least 200% of the calculated stress values.

Table (1). Semiconductor Selection

Semiconductor	Voltage Stress	Type of Semiconductor
S_1, S_2	$\frac{V_{o1}}{2}$	IRFP150N V_{DS} = 100V
D_1, D_2, D_3, D_4	$\frac{V_{o1}}{2}$	MBR30100PT V_R=100V

5. Comparison of the Proposed Converter with Other Converters

In recent years, significant focus has been placed on the design of multi-port DC-DC topologies. The main goal is to achieve a structure with the minimum number of elements, low control complexity, and maximum efficiency. Due to the expanding application of these converters in hybrid systems, numerous topologies have been proposed, each with their own advantages and limitations. The comparison here has been conducted based on the number of elements, number of input-output ports, step-up and step-down capability, continuous input current, common ground, independent control of output voltages, potential bidirectional port, and voltage stress on semiconductor elements. The comparison is performed for single-input multiple-output structures.

In the comparison shown in table (2), the designs in [11, 13, 15] and the proposed converter have a similar number of elements, but it should be noted that the step-up voltage gain of the proposed converter is higher compared to the presented works. On the other hand, converters in [11] and [15] do not have a step-down port. The converters in [13] and [15] have higher voltage stress compared to the proposed converter, and

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therefore, these higher stresses lead to the selection of switches with higher voltage stress tolerance. Although the circuits presented in [12, 17, 19, 20] have fewer elements compared to the proposed converter, their limitations such as limited step-up voltage gain, high voltage stress on diodes, and high voltage stress on switches should be taken in consideration. In all the presented converters in table (2), the input currents are continuous, enabling connection to renewable sources feasible. One of the fundamental challenges in multi-port converters is the elimination of leakage and circulating currents. In the proposed design, a common ground between the input and all outputs has eliminated these unwanted currents and simplified the gate driver circuit; a superior feature not observed in [12] and [15]. A very important point in the design of the proposed converter is the existence of independent control of the output ports. Using independent control, the output voltage gain of each output can be controlled by its designated switch. The designs in [13, 16] and the proposed converter have the feature of independent control of output voltages. None of the presented structures include a bidirectional port, while in the proposed converter, the second output can be used as a bidirectional port. Therefore, this feature distinguishes the proposed converter from similar presented works.

Table (2). Comparison of the proposed converter with other similar works

References	**Elements**					**Number of ports**	**Boost**	**Buck**	**Voltage gain**	**Common ground**	**Independent control**	**Input current**	**Diode voltage stress**	**Switch voltage stress**	**Bidirectional port Capability**
	Inductor	**Capacitor**	**Diode**	**Switch**	**Total**										
11	2	6	2	2	12	1-2	✓	✗	$V_{o1}=\frac{1+n_1D}{1-D_1}V_{in}$ $V_{o2}=\frac{1+n_2-n_2D}{1-D}V_{in}$	✓	✗	✓	$\frac{V_{o1}}{1+n_1D}$	$\frac{V_{o1}}{1+n_1D}$	✗
12	2	3	2	4	11	1-2	✓	✓	$V_{o1}=\frac{1}{1-D_1-D_2}V_{in}$ $V_{o2}=\frac{D_1-D_2}{1-D_2}V_{in}$	✗	✗	✓	$\frac{V_{o1}}{2}$	$\frac{V_{o1}}{2}$	✗
13	3	3	3	3	12	1-3	✓	✓	$V_{o1}=\frac{V_{DC}}{1-D_1}$ $V_{o2}=\frac{D_2V_{DC}}{1-D_2}$ $V_{o3}=D_3V_{DC}$	✓	✓	✓	V_{o1}	V_{o1}	✗

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15	1	5	5	1	12	1-2	✓	✗	$V_{o1} = \frac{2}{1-D}V_{in}$ $V_{o2} = \frac{1}{1-D}V_{in}$	✗	✗	✓	-	$(1-D)V_{o1}$	✗
16	1	6	6	1	14	1-2	✓	✗	$V_{o1} = \frac{2}{1-D}V_{in}$ $V_{o2} = \frac{1+N}{1-D}V_{in}$	✓	✓	✓	$\frac{V_{o1}}{2}$	$\frac{V_{o1}}{1+D}$	✗
17	2	3	3	2	10	1-2	✓	✓	$V_{o1} = \frac{2-D_2}{1-D_2}V_{in}$ $V_{o2} = [(D_2 - D_1) + (D_1 - D_2)\frac{2-D_2}{1-D_2}]V_{in}$	✓	✗	✓	-	$\frac{V_{o1}}{2-D_2}$	✗
19	1	4	4	1	10	1-3	✓	✓	$V_{o1} = \frac{2-d}{1-d}V_{in}$ $V_{o2} = \frac{dN_B}{1-d}V_{in}$ $V_{o3} = \frac{1+\frac{d}{N_A}}{1-d}V_{in}$	✓	✗	✓	$\frac{V_{o1}}{2-D}$	$\frac{V_{o1}}{2-D}$	✗
20	2	3	3	3	11	1-2	✓	✓	$V_{o1} = \frac{1-D_2}{D_1-D_2}V_{in}$ $V_{o2} = \frac{1}{D_1-D_2}V_{in}$	✓	✗	✓	V_{o1}	V_{o1}	✗
Pro	2	4	4	2	12	1-2	✓	✓	$V_{o1} = \frac{2}{1-D_1}V_{in}$ $V_{o2} = \frac{D_2}{1-D_1}V_{in}$	✓	✓	✓	$\frac{V_{o2}}{2}$	$\frac{V_{o1}}{2}$	Potential extention

6. Control Algorithm for the Proposed Model

As shown in the control algorithm in Fig. 5, the status determined by the selector specifies which operation mode is enabled. If S=1, circuit is in the first operation mode and has both outputs; if S=2, the second operation mode is enabled and only the first output is supplied; and finally, if S=3, the third operation mode is activated and only the second output is supplied. Initially, for the case where S=1, the input power and output powers are calculated. If the input power is greater than the sum of the output powers, we consider the reference voltage value for the first output and the reference voltage value for the second output, and control the outputs with switches 1 and 2. For S=2 and the second operational mode, we compare the input power with the first output power. If the input power can supply the output, the controller is activated for that output. Again, the first output voltage provides the required pulse drive for S1 through the compensator to bring the output closer to the reference value. We have the same process for the third mode. Since the

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number of elements and circuit conditions differ in each mode, we have different control equations for each mode and need the appropriate compensator for each mode. In the first mode, due to the correlation of outputs, to select the appropriate compensator, we achieve the desired compensator through decoupling the control equations. In summary, the selector detects the status; in the next step, we check whether the input power in each mode can supply the output; if so, according to the reference value and appropriate control, we provide the desired pulse with the suitable duty cycle so that the output reaches the specified value.

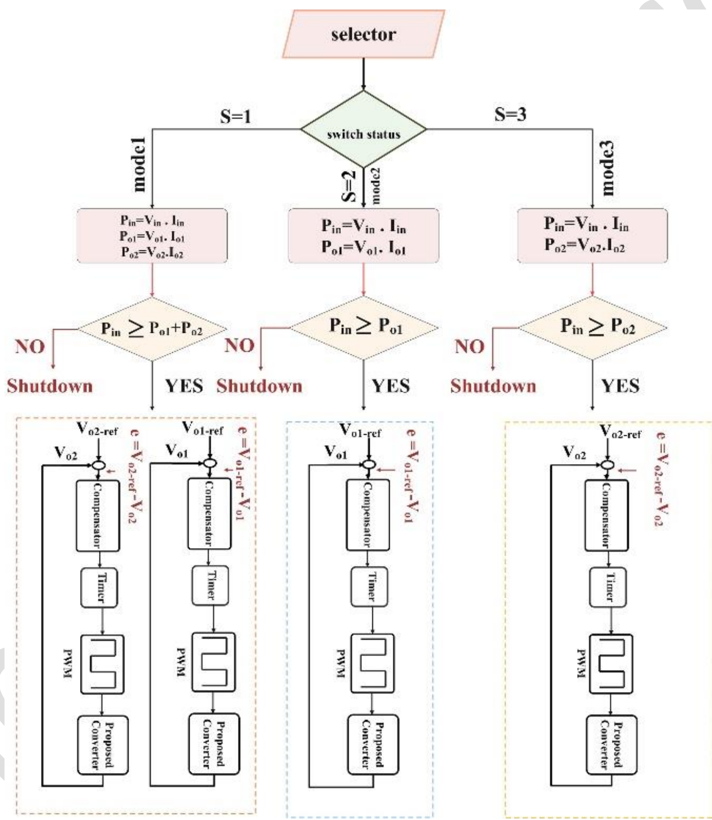

Fig. (5). Control algorithm of the proposed converter

7. Simulation Results

To validate the theoretical analysis and evaluate the performance of the proposed multiport converter, comprehensive simulations are carried out in the PLECS software. The simulation model is configured

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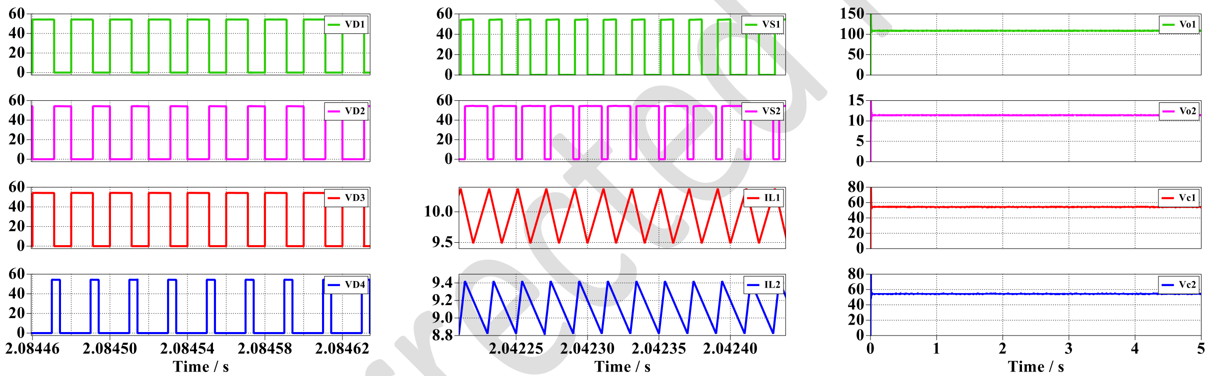
using the designated nominal parameters, featuring an input voltage of $V_{\text{in}} = 24$ V, load resistances of $R_1 = 93$ and $R_2 = 1.25$, and duty cycles fixed at $d_a = 0.56$ and $d_b = 0.21$.

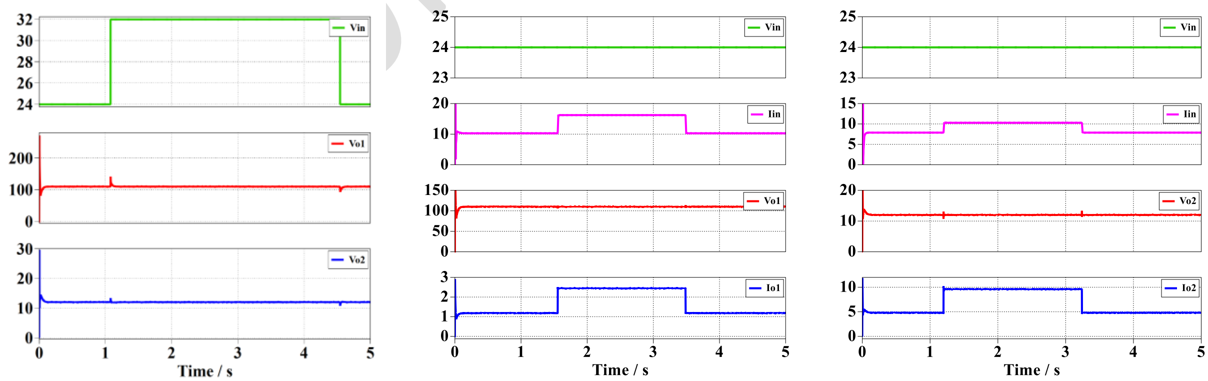
The evaluation is divided into steady-state and dynamic control performance:

- Steady-State Performance: The steady-state waveforms of the proposed converter, including the inductor currents, semiconductor voltage stresses, and output voltages, are illustrated in Fig. 6.
- Dynamic and Control Performance: To demonstrate the robustness of the control strategy and the dynamic response of the converter under transient conditions, the closed-loop simulation results are presented in Fig. 7.



(a) (b) (c)

Fig. 6. Steady-State Performance of Mode 1, (a) Voltage Stress of Diodes, (b) Voltage Stress of switches and Inductor Current, (c) Voltage Stress of Capacitors and Output Voltage.



(a) (b) (c)

Fig. 7. Dynamic and Control Performance of Mode 1, (a) Dynamic response of output voltages (V_{o1}, V_{o2}) under input voltage (V_{in}) step changes between 24V and 32V, (b) Dynamic response of the converter under step load changes in the first output port, (c) Dynamic response of the converter under step load changes in the second output port.

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The steady-state waveforms of the proposed multiport converter under nominal operating conditions are illustrated in Fig. 6. Specifically, Fig. 6(a) illustrates the voltage stress across diodes D_1 to D_4, where it is observed that the voltage stress is identical for all four diodes, with a peak value of 55 V. As depicted in Fig. 6(b), the peak voltage stresses across switches S_1 and S_2 are equal, maintaining a steady value of 55 V, while the average currents flowing through inductors L_1 and L_2 are established at 10 A and 9.1 A, respectively. Furthermore, the voltage waveforms of the capacitors and output ports are illustrated in Fig. 6(c), demonstrating that the voltage stresses on the capacitors are equal to 55 V, while the first and second output voltages are successfully maintained at 110 V and 12 V, respectively.

The performance of the control system under different changes is shown in Fig. 7. As shown in Fig. 7(a), when the input voltage changes from 24 V to 32 V, the control loop quickly fixes this change, and both output voltages return to their reference values without any oscillations. Also, the control performance is tested under sudden load changes. As shown in Fig. 7(b), when the load of the first port changes, the control loop successfully keeps the first output voltage stable at its reference value. This correct performance is also repeated for the second output port in Fig. 7(c), where the second output voltage follows its reference accurately. These waveforms prove that the control strategy ensures good voltage regulation and prevents voltage drop or rise during load changes at both output ports.

8. Experimental Results

The proposed converter was built and tested in the laboratory. Table (3) presents the test conditions and components used for implementing this converter. The test setup is shown in Fig. (8). Furthermore, the necessary pulses for the circuit operation are generated by the STM32F103C8T6 board and applied to the driver circuit. The proposed converter includes three operating modes, all of which have been tested in the laboratory prototype. In the first mode, the simultaneous operation of the output voltages is shown. Fig. (9)(a) displays the voltage stress of the capacitors and the output voltages. According to calculations, the voltage stress values of the first and second capacitors are equal to each other at 56.5 volts. Furthermore,

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the calculated output voltages have values of 110 volts and 12 volts. According to Fig. (9)(a), the measured stress values for the first capacitor, second capacitor, second output voltage, and first output voltage are 52 volts, 56 volts, 11.9 volts, and 111 volts, respectively.

Table (3). Test conditions and components used for implementing the converter

Type	Mosfet	Diode	Inductor	Capacitor	
	IRFP150	MBR30200	400µH	120 µF, 250V	330µF, 100V
Number of components	2	4	2	2	2
Features	First Mode: V_{in} = 24V, V_{o1}=110V, V_{o2}=12V, d_1=0.56, d_2=0.21, R_1=93Ω, R_2=1.25Ω Second Mode: V_{in}=24v, V_{o1}=110V, d_1=0.56, R_1=60.5Ω Third Mode: V_{in}=24v, V_{o2}=12v, d_2=0.5, R_2=1.2Ω				

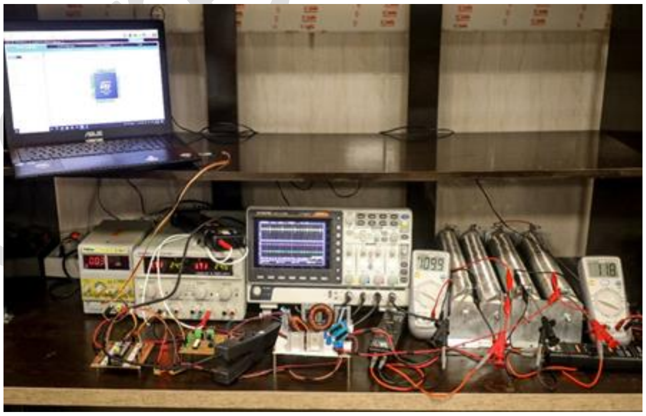

Fig. (8). Laboratory setup for testing the proposed converter

Fig. (9)(b) shows the voltage stress of the diodes in the first mode, where according to calculations, their values are VD1 = VD2 = VD3 = VD4 = 56V, and the measured values in the experimental results for the

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first, second, third, and fourth diodes are 61V, 58V, 61V, and 54V, respectively. The voltage stress values of the switches and the inductor currents are also shown in Fig. (9)(c).

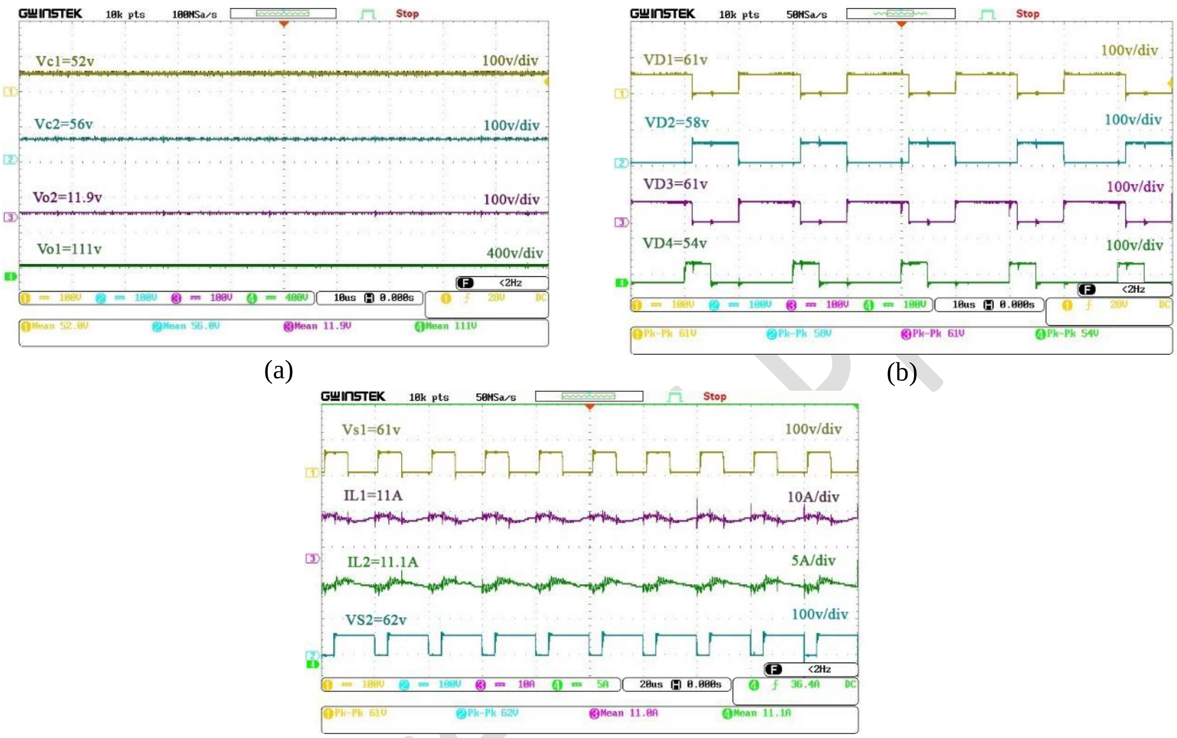

Fig. (9). Test conditions for input voltage of 24 V, first output voltage of 110 V and power of 130 W, second output voltage of 12 V and power of 115 W (a) Capacitor voltages and output voltages in the first mode; (b) Voltage stress of diodes in the first mode; (c) Voltage stress of switches and inductor currents in the first mode

Based on the analytical derivations, simulation outcomes, and experimental measurements, a comprehensive comparative analysis can now be presented to evaluate the designated converter parameters. Table (4) provides a detailed comparison among the calculated theoretical values, the PLECS simulation results, and the measured laboratory data. As observed from the table, the high degree of agreement among the three sets of data firmly validates the accuracy of the mathematical and confirms the practical feasibility of the proposed multiport converter.

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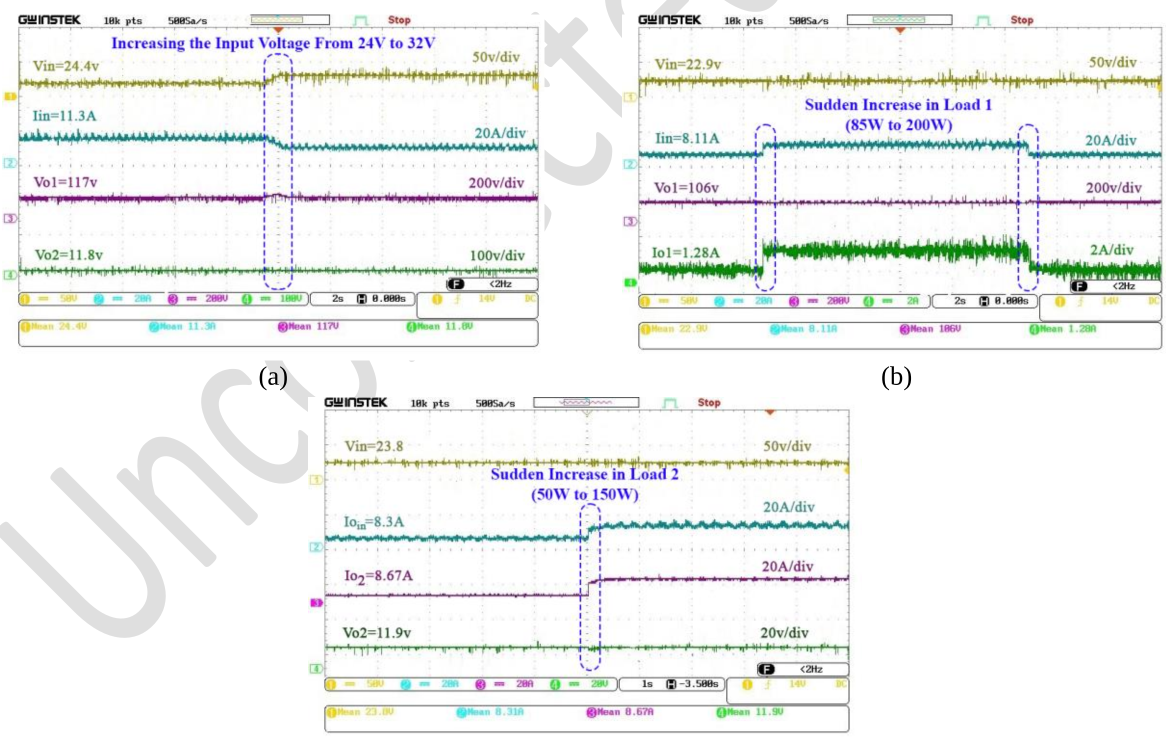
TABLE (4). Comparison of Theoretical, Simulation, and Experimental Results for the Proposed Converter.

Component	Theoretical	Simulation	Experimental Results
S_1, S_2	$\frac{V_{o1}}{2}=\frac{110}{2}=55V$	55V	61V, 62V
D_1, D_2, D_3, D_4	$\frac{V_{o1}}{2}=\frac{110}{2}=55V$	55V	61V, 58V, 61V, 54V
V_{o1}	$\frac{2}{1-D_a}V_{in}\cong 110V$	110V	111V
V_{o2}	$\frac{V_{in}}{1-D_a}D_b\cong 12V$	12V	11.9V

Fig. (10)(a) displays the performance of the proposed converter against input voltage variations. As seen, the input voltage value is changed from 24V to 30V, and the output voltages remain constant at their values, demonstrating the proper performance of the voltage controller against input voltage variations. Fig. (10)(b) displays the controller's performance against an increase in the first output load. As seen, with the increase in output power, the first output voltage remains controlled and follows the reference value. In Fig. (10)(c), with the increase in the second output power, the second output voltage also remains constant, demonstrating the proper performance of the controller under various operating conditions.



(a) (b)

(c)

Fig. (10). Dynamic performance of the proposed converter in the first mode: (a) Dynamic response of the output voltages under an input voltage step change from 24 V to 30 V; (b) Dynamic response of the control system under a

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step load change at the first output port from 85W to 200 W; (c) Dynamic response of the control system under a step load change at the second output port from 50 W to 150 W.

9. Efficiency of the Proposed Converter

To evaluate the overall performance of the proposed multiport converter, an experimental efficiency analysis is conducted across the entire load range. The measured efficiency curve of the developed prototype is illustrated in Fig. 11, which has been integrated into the experimental results to validate the practical performance of the circuit.

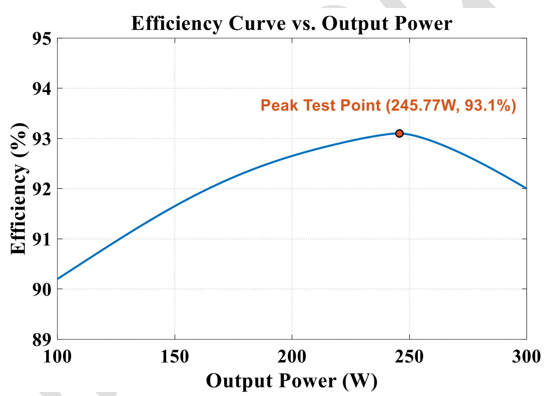

Fig. (11). Measured efficiency curve of the proposed DC/DC converter versus output power.

Under nominal operating conditions, the converter achieves a peak experimental efficiency of 93.1% at an output power of 245.77 W. This peak efficiency point corresponds to an experimental test condition with a measured input power of 264 W (24 V / 11 A input). At this operating point, the first and second output ports deliver power to the load resistances of 93 Ω and 1.25 Ω, maintaining the output voltages at $V_{o1} =$ 111 V and $V_{o2} = 11.9$ V, respectively. These experimental outcomes demonstrate a strong agreement with the theoretical efficiency calculations, thereby confirming the high-efficiency claims and reinforcing the practical credibility of the developed prototype setup.

10. Conclusion

In this paper, a single-input converter with an input voltage of 24 V, simultaneously supplying two outputs of 12 V and 110 V, has been introduced and designed and implemented. The most important features of this converter include the independent control of the outputs, an appropriate number of elements, common ground, continuous input current, suitable voltage gain, and low voltage stress on diodes and switches. A prototype of the proposed model has been built and its performance has been tested in the laboratory at a power of 250 W. The obtained results demonstrate the accuracy of the controller design and the converter's performance.

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