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A New Ultra Step-Up DC–DC Converter with an input continues current for Photovoltaic system

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Abstract

This paper presents a high step-up DC–DC converter with enhanced performance characteristics suitable for low-voltage renewable energy applications. The proposed topology achieves high voltage gain over a wide duty-cycle range without imposing excessive electrical stress on semiconductor devices. Owing to its structural configuration and energy transfer mechanism, the converter exhibits low input current ripple and operates effectively in continuous conduction mode. The voltage and current stresses across the switches and diodes are significantly reduced, allowing the use of lower-rated power devices while maintaining high efficiency. The converter also features a common ground between the input and output terminals, which simplifies gate-driver design, reduces electromagnetic interference, and improves overall system safety. Its structure is straightforward and practical for implementation in renewable energy systems such as fuel cells, photovoltaic modules, and electric vehicle power systems. A 240 W laboratory prototype has been developed to validate the theoretical analysis, achieving a peak efficiency of 93.4% at rated load.

Keywords: Ultra Step-Up, DC-DC converter, Input continues current, Photovoltaic

1- Introduction

The rapid growth of renewable energy systems such as photovoltaic (PV) modules, fuel cells, and battery storage units has intensified the demand for high step-up DC–DC converters capable of interfacing low-voltage sources with high-voltage DC buses or grid-connected inverters [1]–[3]. Since these sources typically operate at low voltage and high current levels, an efficient power conversion stage with large voltage gain, reduced semiconductor stress, and high-power density is essential. However, the conventional boost converter requires extreme duty cycles to achieve high gain, resulting in severe conduction losses, high voltage stress across the switch, and poor efficiency at elevated power levels [4], [5].

To overcome these limitations, switched-capacitor (SC) based converters have been widely investigated due to their ability to provide high voltage gain without magnetic components or with reduced magnetic size [6]–[8]. SC converters achieve gain extension through capacitor charging–discharging sequences and voltage stacking techniques. Although they offer compact size and modularity, they often suffer from high current spikes, increased conduction losses due to multiple series capacitors and diodes, and limited power capability in high-current applications [7], [9]. Moreover, voltage balancing among capacitors and electromagnetic interference (EMI) concerns remain challenging in practical implementations [10].

Coupled-inductor (CI) based converters represent another attractive solution for high step-up applications [11]–[13]. By introducing magnetic coupling and turns ratio extension, these converters achieve quadratic or even higher voltage gain while maintaining moderate duty cycles. Furthermore, the leakage inductance of coupled inductors can be exploited to mitigate diode reverse recovery and enable soft-switching conditions [12], [14]. Despite these advantages, CI-based structures generally require careful magnetic design, and excessive turns ratio may increase leakage energy, core losses, and winding complexity [15]. Additionally, multi-winding coupled inductors increase fabrication difficulty and may reduce reliability in high-power applications.

Quadratic boost converters (QBCs) and cascaded topologies have also been extensively reported to enhance voltage gain without operating at extreme duty cycles [16]–[18]. These structures effectively multiply the

gain of classical boost converters and can be combined with SC cells or CIs for further extension. Nevertheless, cascaded configurations typically increase the number of active switches and passive components, which leads to higher cost, increased control complexity, and reduced power density [17], [19].

Isolated high step-up converters, including flyback, forward, push–pull, and full-bridge topologies, provide galvanic isolation and flexible voltage scaling via transformer turns ratio [20]–[22]. Isolation improves safety and eliminates ground-loop issues, which is especially important in grid-connected systems. However, isolated converters usually experience higher transformer losses, increased leakage inductance, complex snubber requirements, and reduced efficiency at high switching frequencies [21], [23]. In addition, transformer design significantly affects system volume and thermal management.

Hybrid structures combining SC networks, coupled inductors, and voltage multiplier cells (VMCs) have recently attracted considerable attention [24]–[26]. These converters aim to achieve ultra-high gain while reducing semiconductor voltage stress and improving efficiency. Some advanced designs integrate active clamp circuits to provide zero-voltage switching (ZVS) for switches and zero-current switching (ZCS) for diodes, thereby reducing switching losses and reverse-recovery problems [14], [25], [27]. Although such approaches improve efficiency, they may introduce additional auxiliary switches, resonant components, and control constraints.

Another critical challenge in high step-up converters is the trade-off between voltage gain and normalized total voltage stress (NTVS) across semiconductors [11], [18], [24]. Increasing voltage gain through additional multiplier cells or higher turns ratios often leads to increased diode count and cumulative conduction losses. Moreover, many high-gain converters exhibit right-half-plane (RHP) zeros in their small-signal models, complicating controller design and degrading dynamic performance under load and input variations [13], [16].

Therefore, despite the extensive development of SC, coupled-inductor, quadratic, cascaded, and isolated high step-up converters, achieving an optimal balance among ultra-high voltage gain, low component count,

reduced voltage stress, high efficiency, manageable control complexity, and high power density remains an open research challenge [1]–[27]. Future converter topologies must carefully integrate magnetic coupling, capacitive voltage multiplication, and soft-switching techniques while minimizing passive element volume and maintaining robust dynamic response.

2- The proposed ultra step-up converter

The presented topology is an ultra-high step-up DC–DC converter that combines a primary boost stage with a secondary voltage-multiplying network to achieve very high voltage gain. In the first stage, inductor L_1, switch S_1, diode D_1, and capacitor C_1 form a conventional boost cell that provides an initial voltage elevation from the low input source. The second stage, composed of inductor L_2, switch S_2, diode D_2, and the intermediate capacitors (such as C_2 and C_4), transfers energy to a cascaded diode–capacitor multiplier network including D_3–D_7 and capacitors C_3, C_5, C_6, and C_7. During switching operation, the capacitors are charged in specific intervals and stacked in series at the output, resulting in a significantly increased output voltage across the load Ro. The intermediate capacitors provide energy buffering and voltage balancing between stages, while the diode network ensures unidirectional energy transfer and sequential voltage boosting. This multi-stage structure enables high voltage gain at moderate duty cycles and distributes voltage stress across multiple components, making it suitable for low-voltage renewable energy applications requiring high DC bus levels.

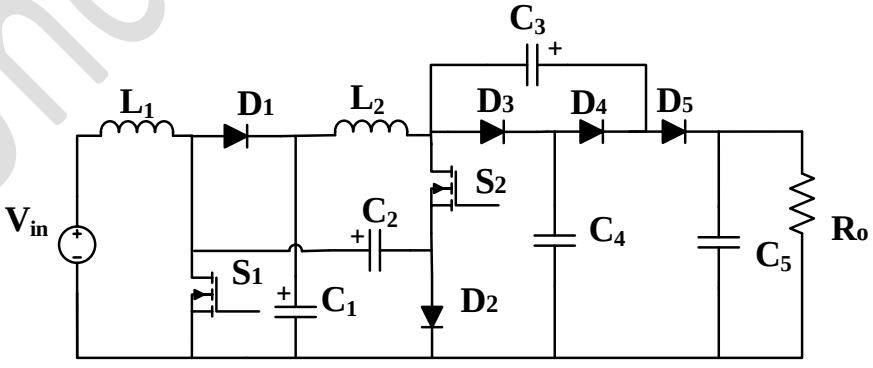

Fig. 1. The schematic of the proposed converter

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For steady-state analysis, one switching period is divided into two main operating intervals. To simplify the analytical derivation, the following assumptions are considered: all semiconductor devices are ideal (zero forward voltage drop and zero switching loss), inductors and capacitors are lossless, the converter operates in continuous conduction mode (CCM), capacitor voltage ripples are small and therefore their voltages can be assumed constant within one switching cycle, and the input voltage is constant. Under these assumptions, the circuit behavior can be clearly described through two dominant operating states within each switching period.

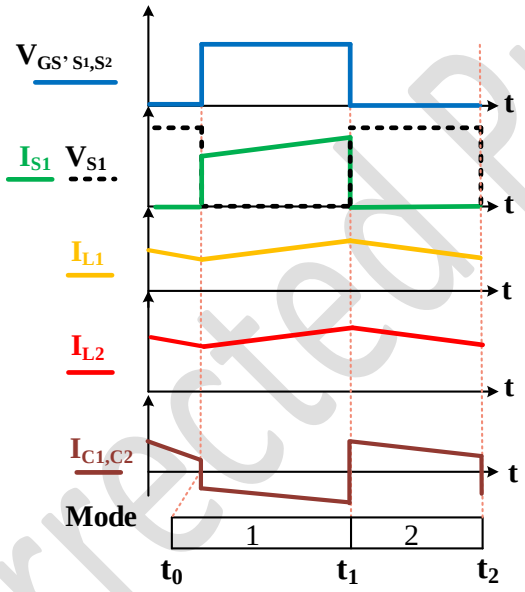

Fig. 2. Key waveforms of the proposed converter

Mode I: In this interval, switches S_1 and S_2 are turned on, and diode D_4 is forward-biased, while all other diodes are reverse-biased. Inductors L_1 and L_2 are charged linearly; L_1 is energized directly from the input source, whereas L_2 is charged through capacitor C_1. During this interval, capacitor C_5 supplys the load current. As a result, the energy is temporarily stored in inductors L_1 and L_2 while the output is supported by the previously charged capacitors.

Mode II: This interval begins when switches S_1 and S_2 are turned off. Immediately, diodes D_1, D_2, D_3, and D_5 become forward-biased. In this state, capacitors C_1 and C_2 are charged through inductor L_1, while

capacitors C_4 and C_5 are charged by inductor L_2. Consequently, inductors L_1 and L_2 release their stored energy and discharge linearly. This interval continues until switches S_1 and S_2 are turned on again, marking the end of the second state and the beginning of a new switching cycle.

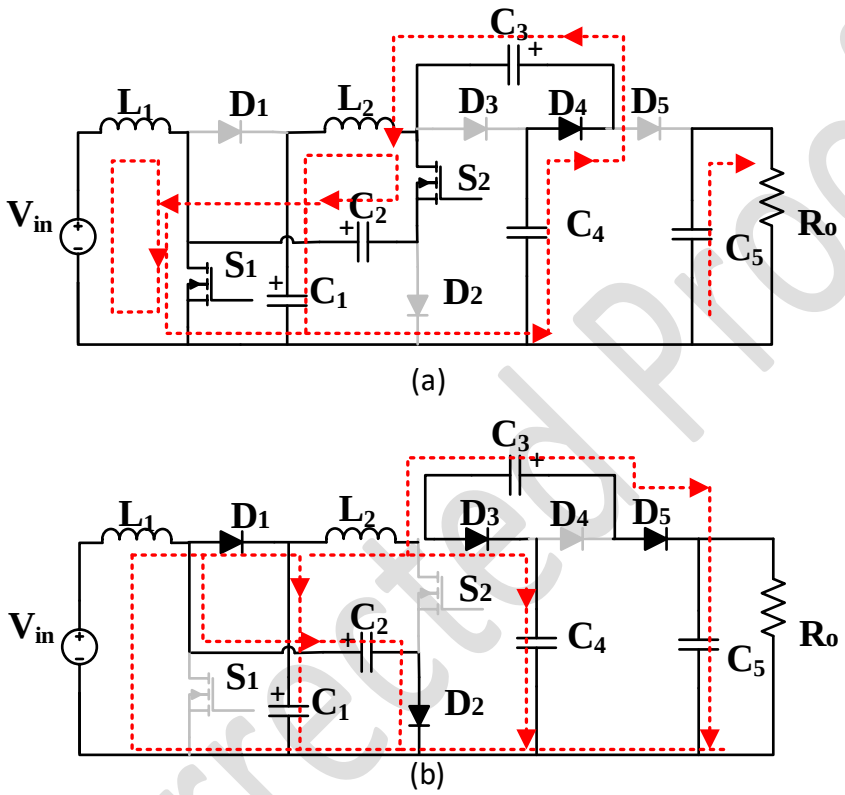

Fig. 3. The equivalent circuits of the proposed converter (a) Mode I (b)Mode II

3- Analysis of the Proposed Converter

In this section, the voltage gain of the converter and the voltage stress across the semiconductor devices are first derived. Subsequently, the design procedure for the inductors and capacitors of the converter is presented.

3-1 Voltage Gain

By applying the volt–second balance principle to inductor L_1, the voltage of capacitor C_2 can be readily obtained. Similarly, by writing the volt–second balance equation for the magnetizing inductor L_m, the voltages of capacitors C_1 and C_3 are calculated. Finally, using these capacitor voltage expressions, the overall voltage gain of the converter is derived. Figure 4 illustrates the voltage gain of the proposed converter for different values of the duty cycle D.

$$v_{L1(\mathrm{ON})}DT + v_{L1(\mathrm{OFF})}(1-D)T = 0 \tag{1}$$

$$V_{in}DT + (V_{in} - V_{C2})(1-D)T = 0 \tag{2}$$

$$v_{L2(\mathrm{ON})}DT + v_{L2(\mathrm{OFF})}(1-D)T = 0 \tag{3}$$

$$(V_{C1} + V_{C2})DT + (V_{C1} - V_{C4})(1-D)T = 0 \tag{4}$$

$$V_{C1} = V_{C2} = \frac{V_{in}}{1-D} \tag{5}$$

$$V_{C3} = \frac{2V_{in}}{(1-D)^2} \tag{6}$$

$$V_{C4} = \frac{V_{in}(1+D)}{(1-D)^2} \tag{7}$$

$$V_O = V_{C5} = V_{C4} + V_{C3} \tag{8}$$

$$G = \frac{V_0}{V_{in}} = \frac{3+D}{(1-D)^2} \tag{9}$$

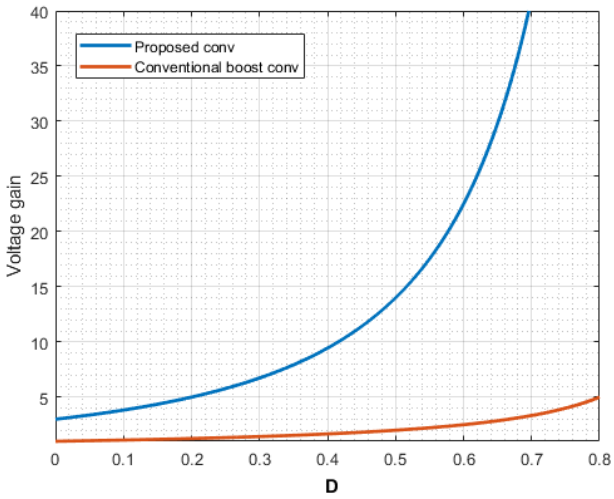

Fig. 4. Voltage gain of the proposed converter in comparison with conventional boost one

3-2 Voltage stress on the semiconductor devices

To calculate the voltage stress across the components, a Kirchhoff's Voltage Law (KVL) equation should be written for the corresponding loop when the device is in the OFF state. In this interval, the blocked switch or reverse-biased diode must withstand the potential difference imposed by the surrounding energy-storage elements, such as inductors and capacitors. Therefore, by identifying the conduction path of the remaining devices and applying KVL around the loop that includes the OFF element, the voltage across that device can be expressed in terms of the capacitor voltages and the input/output voltages. Figure 5 illustrates the normalized voltage stress of the switches and diodes. As can be observed, with an increase in the duty cycle, the voltage stress across switch S_1 and diodes D_3 to D_7 decreases, whereas the voltage stress of switch S_2 increases. Therefore, it is preferable to limit the duty cycle to the range of approximately 0.4–0.5 in order to maintain low voltage stress across all semiconductor devices.

$$V_{S1} = V_{C1} = \frac{V_{in}}{1-D} \tag{10}$$

$$V_{S2} = V_{C4} = \frac{V_{in}(1+D)}{(1-D)^2} \tag{11}$$

$$V_{C1} = V_{D1} = V_{D2} = \frac{V_{in}}{1-D} \tag{12}$$

$$V_{D3} = V_{D4} = V_{D5} = V_{C3} = \frac{2V_{in}}{(1-D)^2} \tag{13}$$

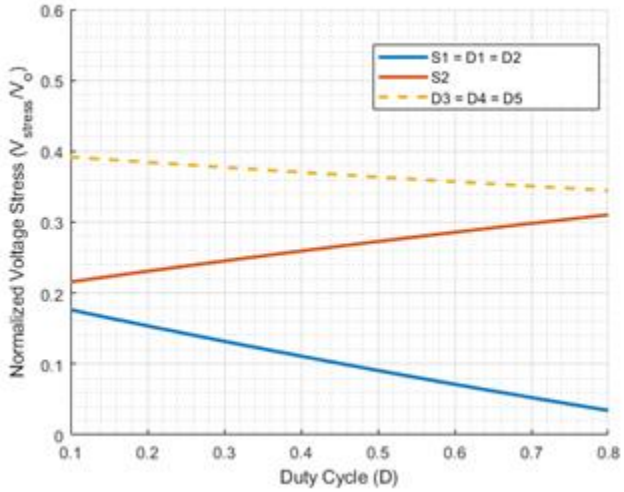

Fig. 5. Normalized voltage stress of the semiconductor devices in the converter

3-3-Design passive elements

In this section, the design equations for the passive components are derived using the fundamental voltage–current relationships of inductors and capacitors. By employing the inductor law, the required inductance values are determined based on the specified current ripple, switching frequency, and the voltage applied across each inductor during the corresponding switching intervals. Similarly, using the capacitor law, the capacitance values are calculated according to the allowable voltage ripple, the charging and discharging currents, and the duration of the conduction intervals.

$$L_1 \frac{di_{L1}}{dt} = V_{in} \Rightarrow L_1 = \frac{V_{in} D}{f_s \Delta L_1} \tag{14}$$

$$L_2 \frac{di_{L2}}{dt} = V_{C1} + V_{C2} \Rightarrow L_2 = \frac{2V_{in} D}{f_s \Delta L_2 (1-D)} \tag{15}$$

$$I_{C1} = C_1 \frac{dV_{C1}}{dt} \Rightarrow C_1 = \frac{(3+D)I_0}{2(1-D)} \frac{1}{f_s R \Delta V_{C1}} \tag{16}$$

$$I_{C2} = C_2 \frac{dV_{C2}}{dt} \Rightarrow C_2 = \frac{(3+D)I_0}{2(1-D)} \frac{V_0 D}{f_s R \Delta V_{C2}} \tag{17}$$

$$C_{3-5} = \frac{V_0 D}{(1-D)} \frac{1}{f_s R \Delta V_{C3-5}} \quad (18)$$

3-4- Discontinuous Conduction Mode (DCM) Analysis

In addition to continuous conduction mode (CCM), the proposed converter may operate in discontinuous conduction mode (DCM) under light-load conditions. In DCM operation, the current of inductor L_1 decreases to zero before the beginning of the next switching cycle. Consequently, each switching period consists of three intervals: the charging interval DT the energy-transfer interval D_1T, and the zero-current interval D_2T, where $D+D_1+D_2=1$.

During the switch-on interval, the current of L_1 increases linearly from zero to its peak value. The peak inductor current can be obtained as

$$I_{L1,pk} = \frac{DV_{in}}{L_1 f_s} \quad (19)$$

Since the inductor current exhibits a triangular waveform in DCM, the average output current is equal to the area of the discharge current waveform over one switching period. Therefore,

$$I_o = \frac{1}{2} D_1 I_{L1,pk} \quad (20)$$

Substituting the peak current expression yields

$$D_1 = \frac{2 I_o L_1 f_s}{DV_{in}} \quad (21)$$

Using the condition $D+D_1+D_2=1$, the duration of the zero-current interval can be expressed as

$$D_2 = 1 - D - \frac{2 I_o}{I_{L1,pk}} \quad (22)$$

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Substituting the above expression into the voltage conversion ratio of the proposed converter results in the DCM voltage gain given by

$$\frac{V_o}{V_{in}} = \frac{3 - D + \frac{2I_o L_1 f_s}{DV_{in}}}{\left(1 - D - \frac{2I_o L_1 f_s}{DV_{in}}\right)^2} \tag{23}$$

It can be observed that, unlike the CCM voltage gain, the DCM conversion ratio depends not only on the duty cycle but also on the inductance value, switching frequency, and load current. Therefore, the converter exhibits a load-dependent voltage gain characteristic in DCM operation. This feature should be considered when designing the controller and selecting the passive components to ensure stable operation over a wide load range.

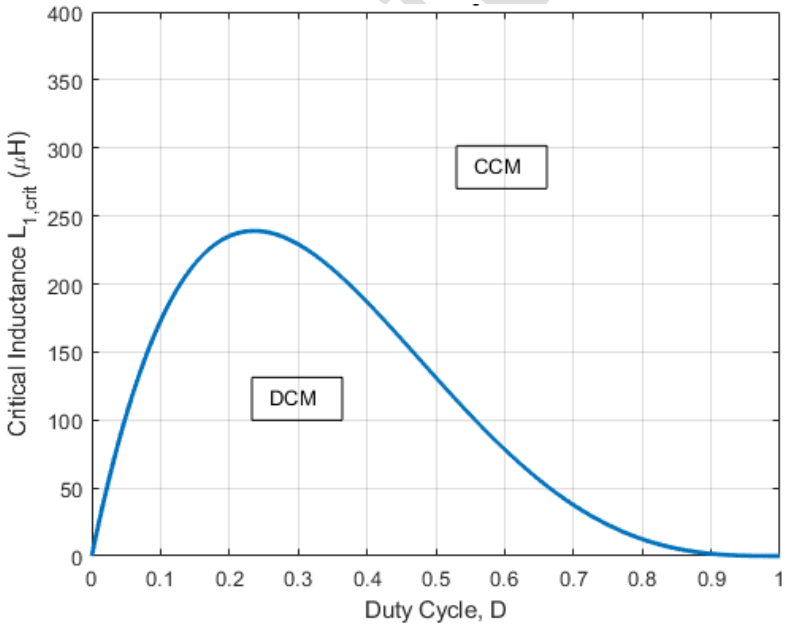

Fig. 6. DCM/CCM boundary inductance L_1

4- LOSS ANALYSIS

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To evaluate the efficiency of the proposed converter, the power losses associated with semiconductor devices, magnetic components, and capacitors are analytically investigated. The total power loss consists of switch conduction losses, switch switching losses, diode conduction losses, inductor copper and core losses, and capacitor ESR losses.

The power-switch losses include both conduction and switching losses. The conduction losses are mainly caused by the MOSFET on-state resistance ($R_{DS}(on)$), whereas the switching losses are associated with the overlap of voltage and current during turn-on and turn-off transitions. In this study, the values of $R_{DS}(on)$, rise time t_r, and fall time t_f are extracted from the datasheet of the selected MOSFET (IPP076N15N5). Accordingly, the total switch loss is calculated using the RMS current and switching parameters of each device.

$$P_{S,cond} = R_{DS(on)}\left(I_{S1,rms}^2 + I_{S2,rms}^2\right) = 0.0076\left(12.4^2 + 4.2^2\right) = 1.30\,\text{W} \quad (24)$$

$$P_{S,sw} = \frac{1}{2} f_s \left[V_{S1} I_{S1}(t_r + t_f) + V_{S2} I_{S2}(t_r + t_f)\right] = \frac{1}{2}(50\times10^3)\left[(60)(12.4)(10\times10^{-9}) + (180)(4.2)(10\times10^{-9})\right] = 0.38\,\text{W} \quad (25)$$

The diode losses are primarily due to the forward voltage drop during the conduction interval. Since the forward voltage of a Schottky diode varies with the conduction current, the forward voltage drop of each diode is determined from the manufacturer's datasheet (VS-20CTQ150-M3) according to its calculated average current. Therefore, the diode conduction loss is obtained as the product of the corresponding forward voltage drop and average diode current, resulting in a more accurate estimation of semiconductor losses.

$$P_D = V_{F,D1} I_{D1} + V_{F,D2} I_{D2} + V_{F,D3} I_{D3} + V_{F,D4} I_{D4} + V_{F,D5} I_{D5} = 0.50(4.04) + 0.48(3.52) + 0.40(1.05) + 0.38(0.80) + 0.35(0.57) = 4.63\,\text{W} \quad (26)$$

The losses in the inductors consist of copper losses caused by the winding resistance and core losses associated with the magnetic material. The copper loss is proportional to the square of the RMS inductor current, while the core loss depends on the operating frequency, magnetic flux

density variation, and core characteristics. These losses become increasingly significant at high switching frequencies and elevated power levels.

$$P_{\mathrm{L,cu}} = r_{L1} I_{L1,\mathrm{rms}}^2 + r_{L2} I_{L2,\mathrm{rms}}^2 = 0.025(12.4)^2 + 0.025(10.2)^2 = 6.44\,\mathrm{W} \quad (27)$$

$$P_{\mathrm{L,core}} = 0.60\,\mathrm{W} \quad (28)$$

Capacitor losses are mainly associated with the equivalent series resistance (ESR) of the capacitors. The ESR loss is proportional to the square of the RMS capacitor current and contributes to the overall thermal stress of the converter. The ESR values used in the calculations are selected according to the specifications of the employed capacitors.

$$P_C = r_{C1} I_{C1,rms}^2 + r_{C2} I_{C2,rms}^2 + r_{C3} I_{C3,rms}^2 + r_{C4} I_{C4,rms}^2 + r_{C5} I_{C5,rms}^2 = 0.10(2.20)^2 + 0.12(2.00)^2 + 0.12(1.80)^2 + 0.10(2.10)^2 + 0.12(1.95)^2 = 2.24\,\mathrm{W} \quad (29)$$

Finally, the converter efficiency is calculated from the ratio of output power to the sum of output power and total losses. By combining all loss components, the theoretical efficiency of the proposed converter can be accurately estimated and compared with the experimental results. This analysis provides valuable insight into the dominant loss mechanisms and confirms the high-efficiency performance of the proposed converter. As shown in Fig. 7, the inductor copper losses represent the largest contribution to the overall power dissipation, followed by the diode conduction losses. Owing to the low on-state resistance of the selected MOSFETs and the optimized converter structure, the switch losses remain relatively small. The total calculated loss is 15.59 W, corresponding to a converter efficiency of 93.9% at full load.

$$P_{\mathrm{loss}} = P_{\mathrm{S,cond}} + P_{\mathrm{S,sw}} + P_D + P_{\mathrm{L,cu}} + P_{\mathrm{L,core}} + P_C \quad (30)$$

$$P_{\mathrm{loss}} = 1.68 + 4.63 + 6.44 + 0.60 + 2.24 = 15.59\,\mathrm{W} \quad (31)$$

$$\eta = \frac{P_o}{P_o + P_{\mathrm{loss}}} \times 100\% = \frac{240}{240 + 15.59} \times 100\% = 93.92\% \quad (32)$$

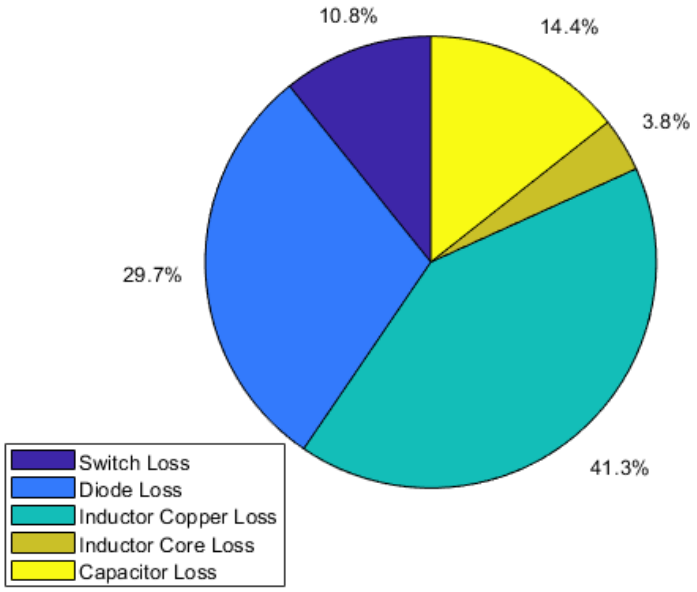

Fig. 7. Distribution of power losses among the main components of the proposed converter at the rated output power of 240 W.

5- Smal signal Analysis

Based on the defined state variables and the averaged matrices, the dynamic behavior of the proposed converter is described using a state-space modeling approach derived from the two switching intervals. The state vector includes the inductor currents and capacitor voltages, while the input corresponds to the source voltage and the output is formed by the summation of the selected output-stage capacitor voltages. The matrices associated with each switching state are obtained by applying Kirchhoff's voltage and current laws to the circuit during the ON and OFF intervals. These mode-dependent matrices are then averaged over one switching period according to the duty cycle to obtain the large-signal averaged model. By linearizing the averaged equations around the steady-state operating point, the small-signal state-space representation is achieved, where the perturbations of the input voltage and duty cycle are explicitly incorporated. This modeling framework enables systematic derivation of the control-to-output transfer functions and provides a solid analytical basis for stability assessment, frequency response evaluation, and controller design of the high step-up converter.

$$\mathbf{x} = \begin{bmatrix} i_{L1} & i_{L2} & v_{C1} & v_{C2} & v_{C3} & v_{C4} & v_{C5} \end{bmatrix}^T \quad (33)$$

$$u = v_g = V_{in} \quad (34)$$

$$v_o = v_{C5} \quad \Rightarrow \quad \mathbf{C_y} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (35)$$

$$\mathbf{A_1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_o C_3} & -\frac{1}{R_o C_3} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_o C_5} & -\frac{1}{R_o C_5} \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{R_o C_5} & -\frac{1}{R_o C_5} \end{bmatrix} \mathbf{B_1} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (36)$$

$$\mathbf{A_2} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & \frac{1}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} \\ \frac{1}{2C_1} & -\frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{2C_2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{2C_3} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{2C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{2C_5} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \mathbf{B_2} = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (37)$$

$$A = DA_1 + (1-D)A_2 \quad (38)$$

$$B = DB_1 + (1-D)B_2 \quad (39)$$

$$\hat{x}' = A\hat{x} + B\hat{v}_g + E_d\hat{d} \quad (40)$$

$$E_d = (A_1 - A_2)X + (B_1 - B_2)V_g \quad (41)$$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = C_y(sI - A)^{-1}E_d \quad (42)$$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{-1.5\times10^4 s^4 + 4.3846153846\times10^9 s^3 - 4.099999999999998\times10^{12} s^2 + 1.356923076923078\times10^{17} s + 1.2000000000000004\times10^{19}}{s^5 + 3.0\times10^1 s^4 + 3.84\times10^8 s^3 + 1.169\times10^{10} s^2 + 7.20\times10^{14} s + 1.80\times10^{16}} \quad (43)$$

The Bode diagram of the uncompensated converter (Fig.8) clearly shows limited phase margin and the presence of high-order dynamics, indicating that the open-loop system cannot ensure stable and well-damped operation without proper compensation.

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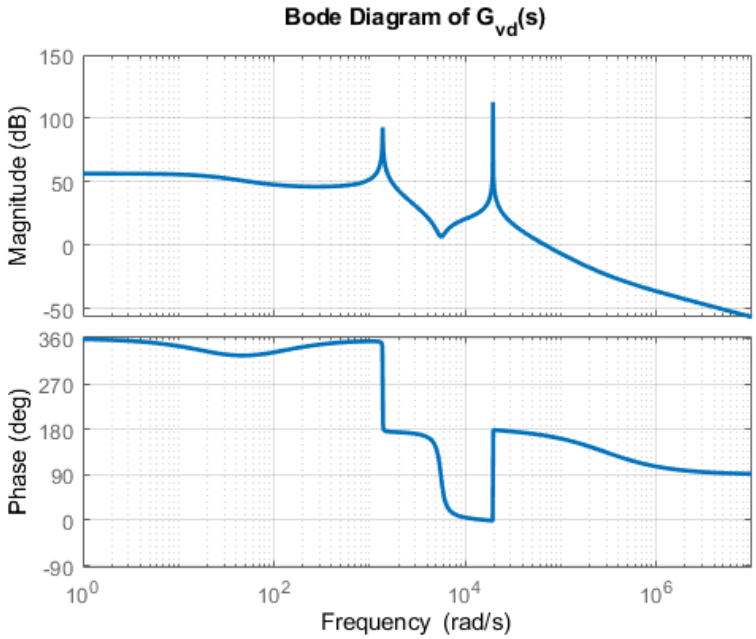

Fig. 8. Diagram bode of $G_{vd}(s)$ without control loop

To improve the dynamic performance and guarantee closed-loop stability, a Type-II compensator is designed for the voltage control loop. The Type-II controller consists of an integrator to eliminate steady-state error, a zero placed near the desired crossover frequency to provide phase boost, and a high-frequency pole to attenuate switching noise and suppress excessive gain at high frequencies. The crossover frequency is selected well below the right-half-plane zero and significantly lower than the switching frequency to maintain sufficient phase margin and avoid interaction with resonant dynamics. The controller gain is then tuned such that the loop gain crosses 0 dB at the chosen frequency while achieving an adequate phase margin, typically above 45–60 degrees.

According Fig. 9 the Bode diagram of the compensated system demonstrates a single well-defined crossover frequency, improved phase margin, and a properly shaped high-frequency roll-off, confirming stable closed-loop behavior and enhanced dynamic performance compared to the uncompensated case.

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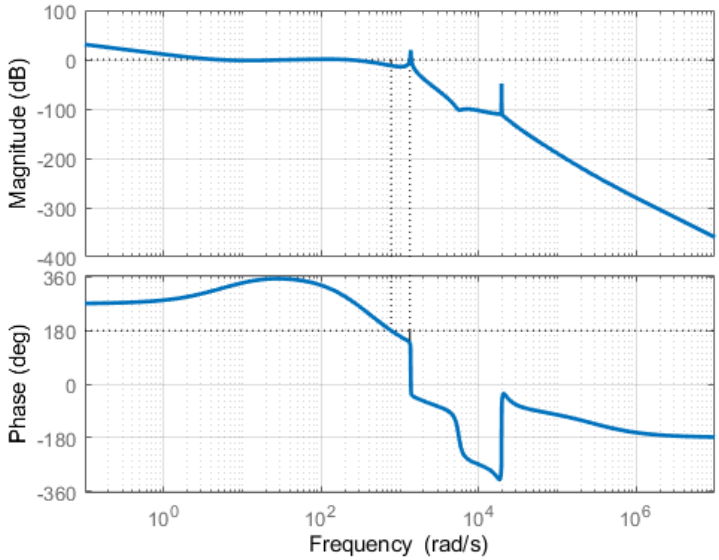

Fig. 9. Diagram bode of $G_{vd}(s)$ with control loop

6- Experimental results

Based on the analytical results presented in the previous section, a detailed simulation model of the proposed converter was first developed in PSpice to verify the theoretical analysis and evaluate the converter performance under various operating conditions. Subsequently, the converter components were designed and a laboratory prototype rated at 240 W was fabricated and tested. The fabricated prototype is shown in Fig. 10, while the calculated values of the converter parameters are summarized in Table 1. Both simulation and experimental investigations were carried out under identical operating conditions to validate the effectiveness of the proposed converter. Also, Fig. 11 illustrates the measured efficiency of the proposed converter under different input-voltage conditions and output power levels. It can be observed that the converter maintains a high efficiency over the entire operating range. As the output power increases, the efficiency gradually improves due to the reduced influence of fixed losses on the overall power

balance. The maximum efficiency of approximately 93.4% is achieved at the rated output power of 240 W. Moreover, the efficiency variation with input voltage is relatively small, indicating that the proposed converter exhibits stable performance under different operating conditions.

Figure 12(a) and (b) present the simulated and experimental voltage and current waveforms of switch S_1, respectively. Likewise, the voltage and current waveforms of switch S_2 are illustrated in Fig. 12(c) and (d), whereas Fig. 12(e) and (f) show the corresponding waveforms of diode D_1. It can be observed that the experimental waveforms closely match the simulation results, confirming the correctness of the converter operating modes and the validity of the theoretical analysis.

Further validation is provided in Fig. 13. The voltage and current waveforms of diode D_2 are shown in Fig. 13(a) and (b), while the current waveform of inductor L_1 is presented in Fig. 13(c) and (d). In addition, Fig. 13(e) and (f) compare the input and output voltages of the converter under the same operating conditions. The results demonstrate that the converter successfully boosts the input voltage from 30 V to approximately 420 V, which is in close agreement with the theoretical voltage-gain prediction.

Although the overall characteristics of the experimental and simulation waveforms are highly consistent, small oscillations and ringing phenomena can be observed in some experimental results, particularly around switching transitions. These oscillations are not visible in the PSpice simulations because idealized component models were employed. In practice, the parasitic inductances of PCB traces and component leads, together with the junction and stray capacitances of semiconductor devices, form resonant circuits that generate high-frequency ringing. Therefore, the observed oscillations are mainly caused by the resonance of parasitic elements and do not affect the normal operation of the proposed converter.

Overall, the close agreement between the analytical, simulation, and experimental results verifies the effectiveness of the proposed converter and confirms its suitability for high-gain DC–DC power conversion applications.

Table 1. Specification of the converter

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Parameter / Component	Value / Specification
Input Voltage, (V_{IN})	30 V
Output Voltage, (V_O)	420 V
Power Switch	IPP076N15N5
Diode	VS-20CTQ150-M3
Inductors, (L_1, L_2)	400 µH
Capacitors, (C_1 – C_5)	47 µF
Output Power, (P_O)	240 W
Switching Frequency, (f_s)	50 kHz

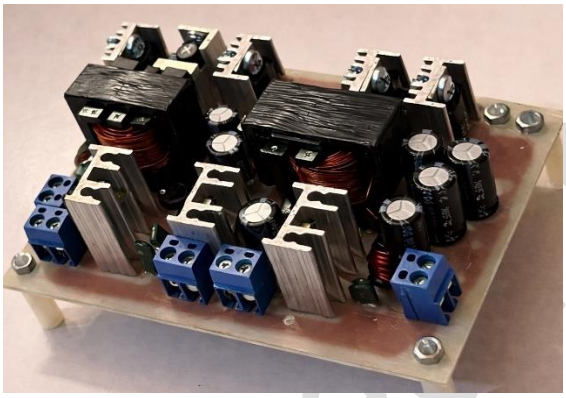

Fig. 10 The photograph of implemented converter

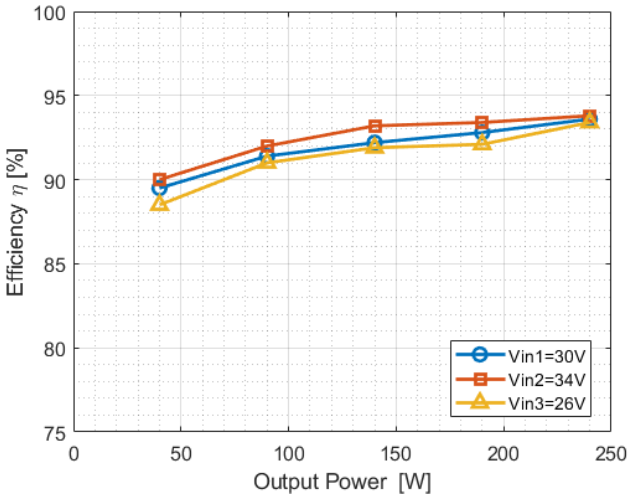

Fig. 11. The efficiency of the converter under various input voltage and output power.

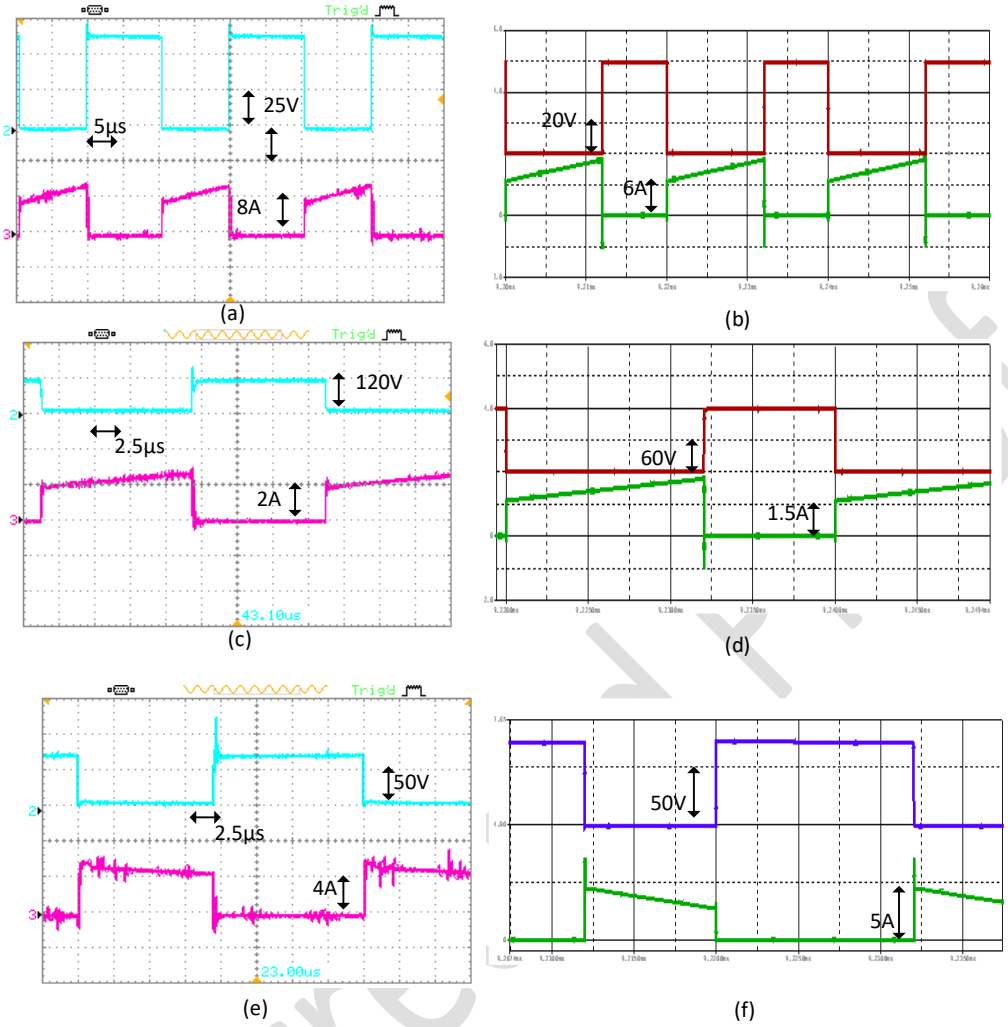

Fig. 12. Experimental and simulation results of the converter (a),(b) Voltage and current of S_1 (c),(d) Voltage and current of S_2 (e),(f) Voltage and current of D_1

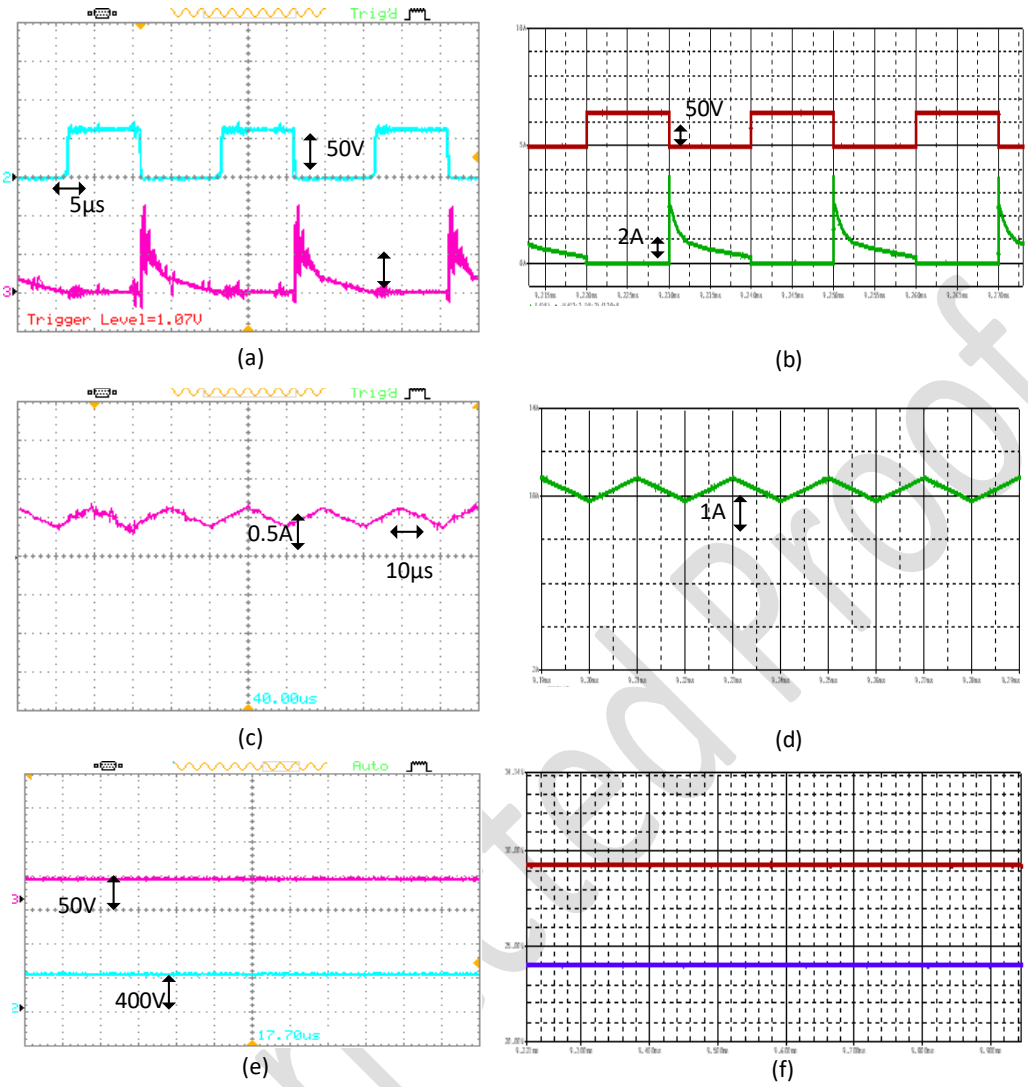

Fig. 13. Experimental and simulation results of the converter (a),(b) Voltage and current of D_1 (c),(d) current of L_1 (e),(f) input and output voltage

The dynamic performance of the proposed converter under load variation is illustrated in Fig. 14. As observed, the output voltage remains tightly regulated without noticeable overshoot, confirming the effectiveness of the controller. The system achieves steady-state operation in less than 200 ms, demonstrating fast transient response. During the load transition, the output current changes from approximately 0.58% of the rated load to the full-load condition of 0.48A, while maintaining stable output voltage regulation. These results validate the robustness of the proposed converter against significant load disturbances.

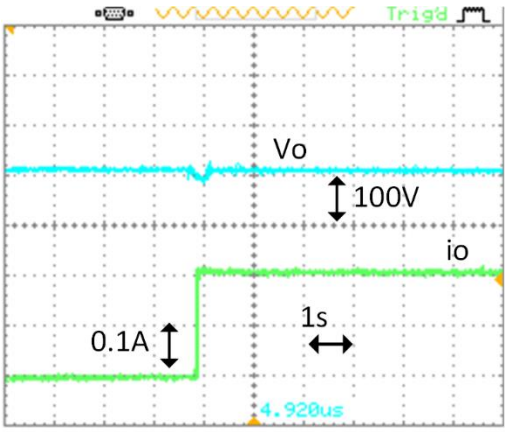

Fig. 14. Dynamic response of the proposed converter under load variation

7- Comparative Analysis

Table 2 provides a detailed comparison between the proposed converter and recently published quadratic DC–DC topologies in terms of voltage gain capability, switch voltage stress, number of elements, input current ripple, common-ground structure, and operating frequency. A number of reported converters achieve high voltage gain; however, this is often accompanied by full output voltage stress on the main switch and high input current ripple, as observed in [18], and [24], which increases semiconductor voltage rating requirements and conduction losses. Several structures reduce switch stress effectively, including [16], [18], and [26], yet these improvements are typically achieved at the cost of increased component count, structural complexity, or the absence of a common-ground configuration, particularly in [16], which may limit their suitability in renewable energy and battery-integrated systems. Soft-switching techniques are adopted in [23] and [26] to enhance efficiency and mitigate switching losses, but they introduce additional control complexity, higher switching frequency in some cases, or isolation requirements. Although low input current ripple is achieved in [17], [20], [22], and [26], several other converters still suffer from high ripple, which can adversely affect source lifetime and EMI performance. In contrast, the proposed converter offers a balanced design by providing high step-up capability together with

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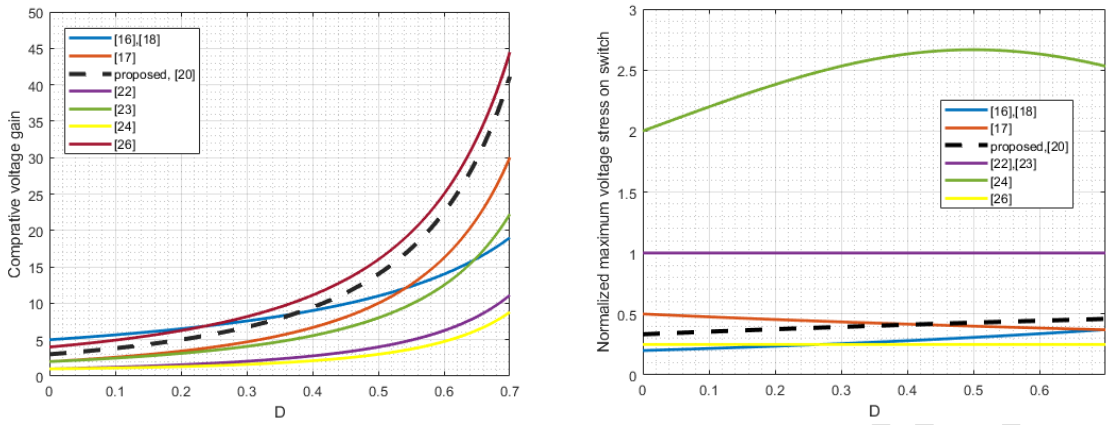
reduced normalized switch stress, low input current ripple, and a common-ground structure, while maintaining a moderate number of elements comparable to other high-gain converters and lower than the most complex topology in the comparison. Furthermore, its rated power level and switching frequency are well aligned with practical medium-power applications, ensuring implementation feasibility without extreme operating conditions. Overall, compared with the converters reported in [16]-[18], [20], [22]–[24], and [26], the proposed topology demonstrates a superior trade-off among gain enhancement, stress reduction, ripple performance, structural simplicity, and practical applicability. Figure 15 shows comparative voltage gain and normalized switch voltage stress.

Table 2. The proposed converter in comparison with similar quadratic converters

1-Magnetic core 2-Total number of elements 3- Common ground



(a) (b)

Fig. 15. Comparative curve (a) comparative voltage gain (b) comparative normalized switch voltage stress

converter	Voltage gain	Maximum voltage stress across switch	No. of elements					CG[3]	Input current ripple	Frequency (kHz)
			S	D	M.C[1]	C	T[2]			
[16]	$\frac{5-4D+D^2}{(1-D)^2}$	$\frac{2V_o}{5-4D+D^2}$	2	5	2	5	14	No	High	50
[17]	$\frac{1+n+D}{(1-D)^2}$	$\frac{V_o}{1+n+D}$	2	4	2	4	12	Yes	Low	50
[18]	$\frac{3-3D+n(2-D)+D^2}{(1-D)^2}$	$\frac{V_o}{3-3D+n(2-D)+D^2}$	2	5	2	5	14	Yes	High	50
[20]	$\frac{1+2n+D}{(1-D)^2}$	$\frac{(1+D)V_o}{1+2n+D}$	2	5	5	2	14	Yes	Low	50
[22]	$\frac{1}{(1-D)^2}$	V_o	2	3	3	3	11	Yes	Low	20
[23]	$\frac{2}{(1-D)^2}$	V_o	1	5	3	3	12	Yes	Low	100
[24]	$\frac{1-D+D^2}{(1-D)^2}$	$\frac{2V_o}{1-D+D^2}$	1	3	3	2	9	Yes	High	50
[26]	$\frac{2+2n}{(1-D)^2}$	$\frac{V_o}{2+2n}$	2	4	3	5	14	Yes	Low	100
Proposed converter	$\frac{3+D}{(1-D)^2}$	$\frac{(1+D)V_O}{3+D}$	2	5	2	5	14	Yes	Low	50

8- Conclusion

The proposed high step-up DC–DC converter demonstrates superior steady-state and dynamic performance, making it a strong candidate for low-voltage renewable energy applications. The converter achieves high voltage gain over a wide duty-cycle range while maintaining reduced voltage and current stress across semiconductor devices. The presence of a common ground between the input and output simplifies the driver circuitry and enhances system safety. Experimental validation using a 240 W prototype confirms the feasibility of the design, with a measured efficiency of 93.4% at rated load. From a stability perspective, the small-signal analysis and closed-loop frequency response evaluation verify stable operation with a phase margin of approximately 50 degrees, ensuring adequate robustness against parameter variations and load disturbances. The compensated system exhibits a single well-defined crossover frequency and properly damped dynamics. Furthermore, the measured input current ripple is approximately 0.5A, which corresponds to nearly 4% of the nominal input current, confirming the low ripple characteristic and the suitability of the converter for renewable sources that require smooth input current profiles.

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