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PV Powered Unified Active Power Filter with Intelligent ANN Controller for PQ Improvement

Vendoti Suresh[1,*], Chinthakula Siva Ganesh[2], Puppala Sri Maha Lakshmi[3], Pilla Manikanta[4] and Simma Saibhaskar[5]

[1]Assistant Professor, Department of Electrical & Electronics Engineering, Godavari Global University, Rajahmundry.

[2]Assistant Professor, Department of Electrical & Electronics Engineering, Godavari Institute of Engineering and Technology (A), Rajahmundry.

[3,4,5] UG Scholar, Department of Electrical & Electronics Engineering, Godavari Institute of Engineering and Technology (A), Rajahmundry.

*Corresponding author: sureshvendoti@gmail.com

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Abstract:

Power quality issues have emerged as one of the most significant problems facing a power system, due to its diverse nature and frequent occurrence. This research introduces a Photovoltaic (PV) incorporated Unified Active Power Filter (PV-UAPF) system and its control approach for generation of decarbonized clean energy and improved Power Quality (PQ). The UAPF, combining shunt and series converter, which is utilized for compensating the current quality and voltage quality issues. Moreover, the PV system is incorporated with Switched Inductor (SI) based Boost-Luo converter at DC link, which is connected between series and shunt converters. For control the operation of converter, PI controller is employed and its parameters are refined by Modified Red Kite Optimization (MRKO) algorithm. For ensuring efficient voltage regulation and to manage the functioning of UAPF, an Artificial Neural Network (ANN) controller is incorporated on load side. To further demonstrate developed work's efficacy, it is implemented in MATLAB/Simulink and comparison is made with existing methods. The outcomes reveals that the developed system has a THD value lower than 5%, ensures the quality of power is enhanced.

Keywords:

PV system, SI based Boost-Luo converter, Modified red kite optimized PI controller, UAPF, ANN controller.

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1. Introduction

Power quality problems are plaguing distribution systems in the era of sophisticated power electronics. Power quality problems are getting worse, which affects both residential and commercial consumers greatly. Customers experience harmonic distortions, inaccurate measurement schemes, malfunctioning protection relays, circuit breakers, and transformer winding heating, among other power quality problems [1- 3]. Power quality difficulties are typically classified into two primary categories: voltage and current quality, which includes harmonic current, current ripple, voltage sag, and voltage swell [4, 5].Power electronics-based Flexible AC Transmission System (FACTS) and controllers provide quick and precise control through a range of electrical system parameters, such as current, voltages, and power flow [6, 7]. PQ enhancement are provided by the FACTS, namely Static Var Compensators (SVC) [8], Thyristor-Controlled Series Compensators (TCSC) [9] and Static Synchronous Compensators (STATCOM) [10]. Nevertheless, they have slower dynamic response, highest cost and complexity. The introduction of Custom Power Devices namely Distribution Static Compensator (DSTATCOM) and Dynamic Voltage Restorer (DVR) provides solution to PQ concerns [11]. Sensitive loads are shielded by DVR, a series variable speed controller, from grid voltage anomalies such dips and surges and flicker interruptions. DVR reduces voltage swell and sag, but if they are not correctly designed and controlled, they induce harmonic distortions into the system [12, 13]. Subsequently, DSTATCOM is a shunt Voltage Source Converter (VSC) that addresses load power quality concerns like load reactive power, current harmonics, etc. Furthermore, it excels in handling circumstances such as sudden load removals and non-linear working conditions. Nevertheless, it is unable to protect the load, from harmonics in the Point of Common Coupling (PCC) voltage [14, 15]. Therefore, this paper develops Unified active power filter for augmentation of power quality. The UAPF is made up of active power filters attached in parallel and series within a standard DC-link. Additionally, it simultaneously resolves all issues related to current and voltage dependent devices. To power the DC link capacitor of UAPF, the PV system is used and its intermittent nature causes fluctuations in grid voltage [16, 17]. Therefore, converter is used and some of the conventional approaches are discussed. A Boost converter is developed in [18, 19] that is ideal for significantly increasing the distributed generation unit’s less input

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DC voltage. On the other hand, large peak currents in a boost converter cause stress and failure in the power transistor. The Buck-Boost converter, which performs both buck and boost mode is designed in [20, 21]. On the other hand, the converter performs poorly at high gain and very small or very large duty cycles. This issues are overcome by using a SI based Boost-Luo converter for boosting the voltage of PV system. To stabilize the voltage PV system, PI controller is utilized and its parameters are tuned by a MRKO algorithm. The main contributions of this work are,

- To reduce voltage fluctuations (voltage swell and sag) and THD, UAPF is exploited, which effectively improves the power quality.
- To control the function of Unified Active Power Filter, ANN controller is exploited.
- To enhance low voltage of PV system, SI based boost-luo converter is exploited.
- To stabilize voltage of PV system, PI controller is used and its parameters are refined by MRKO algorithm.

2. Proposed Methodology

The UAPF safeguards crucial loads connected to distribution system by tackling problems with neutral and negative sequence currents, voltage disturbances, harmonic distortions, reactive power flow at fundamental, and harmonic isolation. This research develops PV powered UAPF with intelligent ANN controller for enhancement of PQ. Fig. 1 represents block diagram of developed research.

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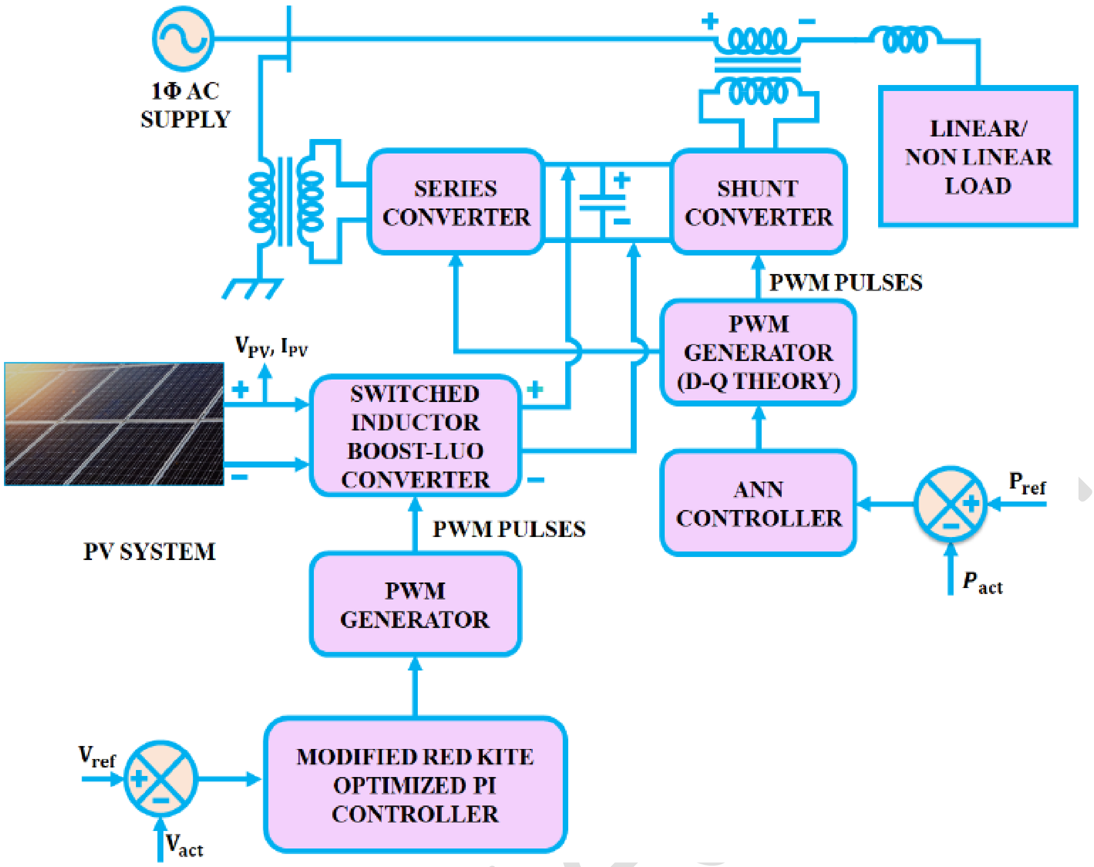

Fig. 1. Block diagram of the proposed PV based DVR work

The low voltage of PV system is boosted by using a SI based Boost-Luo converter. Then, the PWM generator generates pulses for better switching operation of the converter. The converter's voltage is stabilized by utilizing a PI controller and its parameters are tuned by MRKO algorithm. After that, output of developed converter is fed into the series and shunt converter (UAPF), which converts DC supply into an AC supply. This conversion process is crucial for maintaining power quality and ensuring a stable power supply. The DC link capacitor that connects these two converters is dependent on the type of converter that is being used. Voltage swell, sag, interruptions, and harmonics are lessened by the series voltage converter, which also controls the load voltage. The application of a shunt converter reduces line current harmonics resulting from non-linearity in the load. The PWM generator is exploited for better switching operation of UAPF and ANN controller is utilized for controlling the operation of UAPF. Then, the output power of UAPF is passed to linear/nonlinear load through 1ϕ AC supply, assures the reduction in power losses and improvement of power quality.

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2-1- PV system

An implemented PV model, as presented in Fig. 2, is based on single-diode PV model. Single-diode, five-parameter system serves as the foundation for this research. The solar system converts the solar into an electrical energy by PV cells.

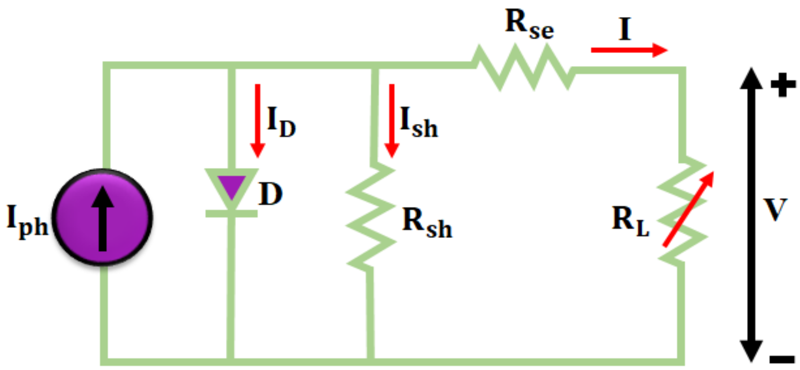

Fig. 2. Circuit diagram of PV model [20]

Derived from the general Shockley equation, the equation (1) represents a basic single-diode model with unique $I-V$ properties.

$$I = I_L - I_O\left[exp\left(\frac{(IR_S)}{a}\right)-1\right]-\frac{(IR_S)}{R_{sh}} \tag{1}$$

Where a is modified ideality factor, R_S is series resistance, R_{sh} is parallel resistance, I_L is lighting diode current and I_O is the diode's reverse saturation current. The primary PV characteristic, shown by the I-V characteristic curve, is described by Equation (1). The low voltage of PV system is enhanced by using SI based Boost-Luo converter.

2-2- SI Based Boost-Luo Converter

Proposed boost-luo converter combines a switching inductor with a Boost and Luo converter. It keeps the DC voltage at the load terminals constant while converting low voltage to high voltage. SI cells actually have unsophisticated structure, strong voltage gain at low duty ratios, uninterrupted input current, low dv/dt switch stress, and high efficacy. They also have minimum spikes at switches and

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reduce leakage currents. The developed converter's high voltage boosting capacity is attained by the utilization of SI cells and low switching elements. Fig. 3 shows the developed converter's circuit diagram. The resistive load R_O is powered by a MOSFET switch (S_{a1}), a SI cell (called SI cell-1), a boosting capacitor (Ca1), a clamping diode(D_{a3}), an output capacitor (C_O), an input inductor(L_i), and an output diode (D_O). Three diodes, (D_{a1} , D_{a2}) and D_{a12}, and two inductors, L_{a1} and L_{a2}, make up SI cell-1.

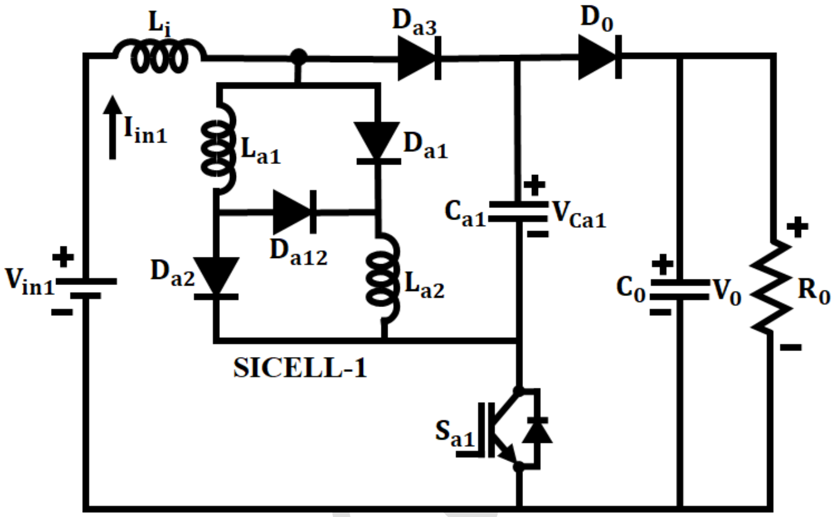

Fig. 3. Proposed converter

The converter architecture produces a persistent output voltage V_O at the load terminals and a greater voltage gain when energized by input DC voltage of V_{in1}. By symmetrically energizing necessary inductors in the SI cell and sequentially switching the switch S_{a1} using the diode at output D_O and capacitor at output C_O, a high voltage is produced at the load terminal.

Mode-I (t0-t1):

In this operating mode-I, gate pulses generated by gate-drive circuitry are sent to switch S_{a1} to turn it on. The input DC voltage V_{in1} charges inductors in SI cells L_{a1}, L_{a2}via SI-cell diodes D_{a1} , D_{a2}, and powers the boost capacitor C_{a1}. By employing the parallel charging technique on switch S_{a1}, some energy has been saved. Voltage across the 2 inductors in L_{a1}, L_{a2} SI cell is VL_{a1}, VL_{a2}, which is same as the DC input voltage of V_{in1}. Current flowing in the capacitor and SI-cell inductors is iC_{a1}, iL_{a1} , and iL_{a2}, which increases linearly, even if the input DC current I_{in1} flows uninterruptedly in the direction of the boost capacitor and inductors of the SI cells C_{a1}, L_{a1} and L_{a2}. Because switch S_{a1} is in the conduction area and reverse-biases the output diode D_O, input DC current not pass to the resistive load. In other words, until the switch S_{a1} enters the non-conduction state, output capacitor C_O continuously sends energy to load R_O while maintaining a constant output voltage V_O. The developed converter's operating mode I is presented in Fig. 4.

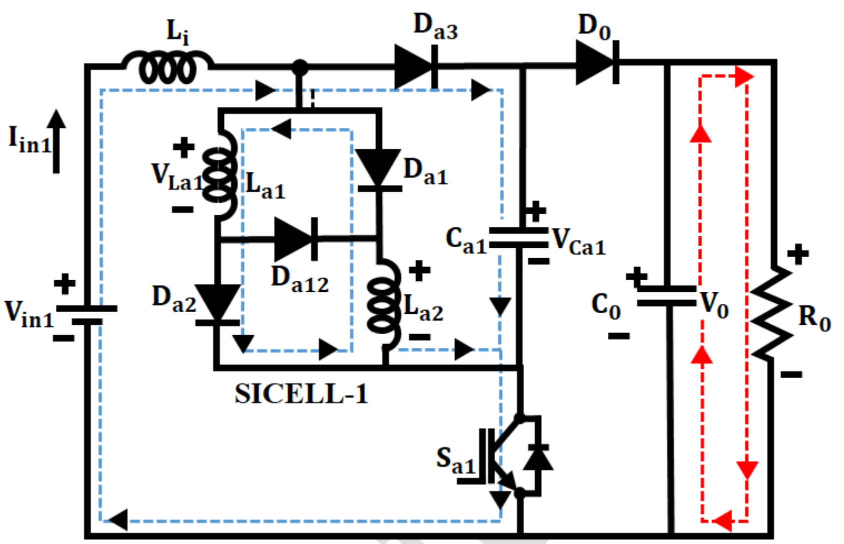

Fig. 4. Mode 1

Mode-II (t1-t2):

By stopping the gate-pulses generated by the gate-drive circuit, switch S_{a1} is switched off in this mode. D_{a12} diode and the D_O output diode are then used to de-energize the energy that is previously stowed in the SI cell-1 inductors L_{a1}, L_{a2} and boost capacitor C_{a1}. With an input voltage of V_{in1}, it used the serial discharge approach to supply energy to a resistive load. Subsequently, voltage across 2 inductors in L_{a1}, L_{a2} SI cell is $-VL_{a1}, -VL_{a2}$ which equivalent to voltage of boost capacitor is in V_{C1}. The load current I_O distributes energy to load and output DC capacitor C_O. While decreasing linearly despite flowing continuously towards the boost capacitors and inductors of the SI cells C_{a1}, L_{a1} and L_{a2}. Because switch S_{a1} is in the non-conduction area and output diode D_O is forward biased, current flows continuously to resistive load, producing a substantial voltage gain at the load terminals. Thus, until switch S_{a1} enters the conduction state, the boost capacitor and switched inductors provide uninterrupted energy to the load R_O while keeping the voltage at output V_O constant.

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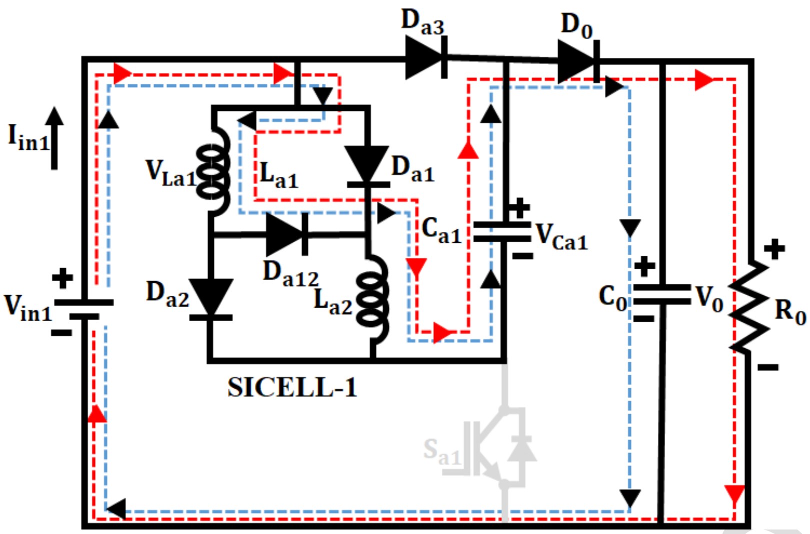

Fig. 5. Mode 2

The working mode II of proposed converter is revealed in Fig. 5. Average voltage induced in switched-inductors is expressed in (2)

$$V_{La1} = V_{La2} = 0 \tag{2}$$

In Mode-I, the quantity of produced voltage and current that flows in SI's are calculated as,

$$V_{La1} = V_{La2} = V_{in1} \tag{3}$$

$$V_{ca1} = V_{in1} \tag{4}$$

$$I_{La1}(t) = I_{La2}(t) = \frac{V_{in1}}{L} \tag{5}$$

In Mode-II, the amount of produced voltage and current that flows in the load are estimated as,

$$V_{in1} - V_{La1} - V_{La2} + V_{ca1} - V_O = 0 \tag{6}$$

According to switch-off period, induced voltages are denoted as,

$$V_{La1} = V_{La2} = \frac{3V_{in1} - V_O}{2} \tag{7}$$

Based on volt-sec balancing principle among the switched inductors L_{a1} and L_{a2}, which is denoted as

$$V_{in1}DT + \frac{3V_{in1} - V_O}{2}(1-D)T = 0 \tag{8}$$

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Voltage gain ratio is

$$\frac{V_O}{V_{in1}} = \frac{4-D}{1-D} \tag{9}$$

Final voltage gain is

$$VG_{CCM} = \frac{V_O}{V_{in}} = \frac{4-D}{1-D} \tag{10}$$

The output of the converter is not constant and have variations because of the irregular nature of the PV system so PI controller is preferred for stabilizing output of converter and its parameters are tuned by MRKO.

2-3- Modified Red Kite Optimized PI Controller

The MRKO is a novel algorithm motivated by the social behaviours of red kites, which is exploited to optimize PI controller's parameters in this research. MRKO starts by producing an initial population of red kites, indicating distinct potential solutions with random locations in the search space. These positions are iteratively updated with each kite indicating a possible solution to the optimization issue. The process of optimization progresses via 2 main stages: exploitation and exploration. In the exploration stage, the red kites search for new regions of search space utilizing both social and individual components (depending upon the unity and danger behaviours). The algorithm exploits coefficients that gradually reduce the entire iterations, balancing among exploration (diverse solutions searching) and exploitation (refining solutions in promising regions). For every iterations, the red kite's positions are updated utilizing the below equations:

Initial position of the red kite

$$Posi,j(t) = lb + rand \times (ub - lb) \tag{11}$$

Where, $Posi,j(t)$ is the position at iteration i and lower and upper bounds are specified by lb and ub.

Selection of leaders

$$Best(t) = Posi(t) \quad \text{If } f_i(t) < f_{best}(t) \tag{12}$$

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When the evaluation function is enhanced the best position is updated.

Position update

$$posnew_i\left(t+1\right)=Posi\left(t\right)+Pmi\left(t+1\right) \quad (13)$$

$$Pmi\left(t+1\right)=D\left(t\right)\times Pmi\left(t\right)\times SC\left(t\right)\times\left(\left(Posrws\left(t\right)-Posi\left(t\right)\right)+UC\left(t\right)\times\left(Best\left(t\right)-Posi\left(t\right)\right)\right) \quad (14)$$

Where, random vectors indicating individual and social components are represented by $SC(t)$ and $UC\ (t)$ and $D(t)$ is a coefficient that reduces over time. The MRKO is exploited to avoid local minima traps and ensure a search space's full exploration, refining the rate of convergence and accuracy of PI controller tuning.

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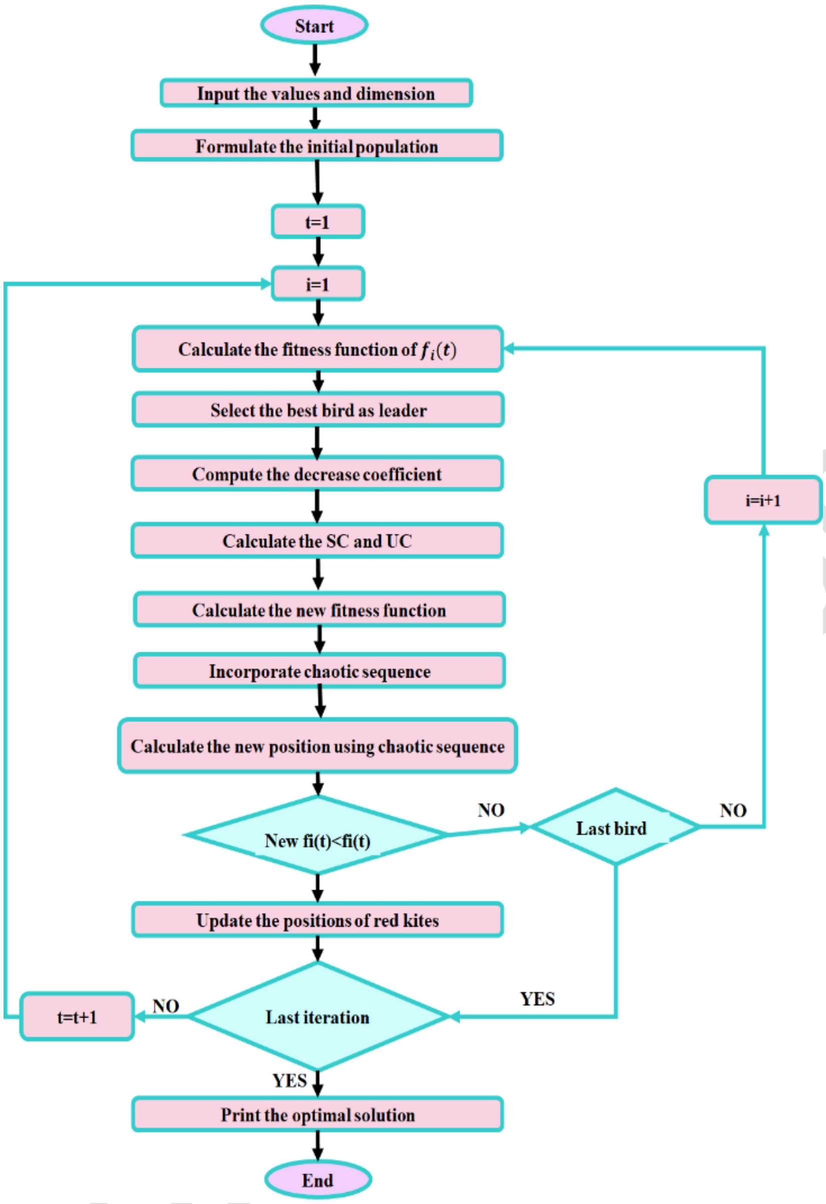

Fig. 6. Flowchart of developed controller

This optimization method assures effective control of DC/DC converter, improving stability of system and performance under varying conditions. Fig. 6 depicts the flowchart of developed controller. Then, output of MRKO-PI controller is given to UAPF that is combination of shunt and series converter.

2-4- Unified Active Power Filter

A system setup for the UAPF uses both shunt and series converters, shown in Fig. 7. Reactive power and harmonics are two current-related problems that a shunt converter mostly corrects for. Voltage-related issues containing voltage swell, sag, and harmonics are the focus of a series converter. Because

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of its ability to handle power quality issues that arise in electrical distribution networks, the UAPF has seen significant development in recent years. Between the utility and its industrial loads, the UAPF offers total and direct isolation against reactive power, harmonic distortions, harmonic currents, and imbalanced circumstances.

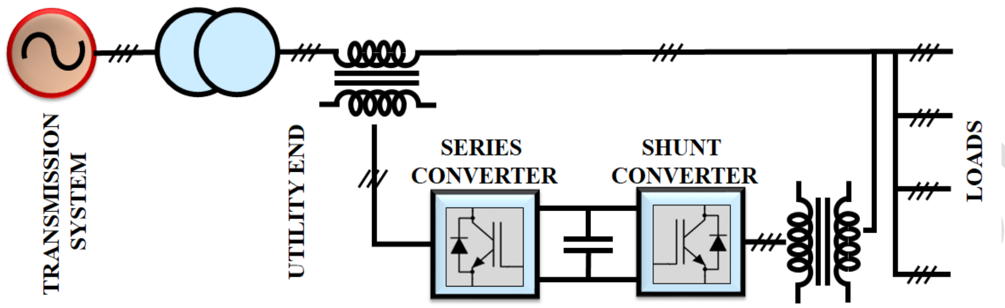

Fig. 7. Structure of UAPF

Shunt Converter

One of the main ways that the PV-UAPF reduces current-based problems of power quality like current harmonics, uneven loading, compensation of reactive power, and low power factor is by connecting shunt converter in the side of load, as illustrated in Fig. 8. Furthermore, it keeps the DC voltage control over the DC link intact and feeds actual solar PV power into utility load and grid. Fig. 7 presents the circuit of shunt converter. Generating reference current pulses and signals for VSC is main job at hand. Equation (15) yields reference DC voltage(V_{dcref}). Equation (16) is utilized to calculate the voltage sag and swell conditions that determine gain K values.

$$V_{dcref} = 3V_{sa} \times \left[1 + \left(K_1 \times K \times 0.1\right)\right] \tag{15}$$

The value of K is 1, when $K_2 \geq 1.02$ and K is 0, when$K_2 \leq 0.98$. Gains values of K_1 and K_2 are estimated as

$$K_1 = \frac{V_{Lm} - V_{Sm}}{V_{Lm}}, K_2 = \frac{V_{Lm} - V_{Sm}}{V_{Lm}} + 1 \tag{16}$$

Where, V_{Lm} and $V_{Sm}$are maximum limit of magnitudes of load and source voltage, which is estimated as

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$$V_{Sm}=\sqrt{\frac{2}{3}\left(V_{Sa}^2+V_{Sb}^2+V_{Sc}^2\right)},V_{Lm}=V_{La}\times\sqrt{2} \tag{17}$$

Where V_{La} and V_{sa} are load and source voltages for every phase 'a'.

After passing via a low-pass filter, the identified DC link voltage V_{dc} is compared to reference DC voltage. Attained error is subjected to PI controller to produce current's loss component. Multiplying loss component of current by DC link voltage yields power loss component (P_{dc}) resulting from DC voltage control. Lastly, Equation (18) provides the overall power (P1) to be taken from the grid.

$$P_1=P_{dc}+P_L-P_{PV} \tag{18}$$

The basic positive sequence powers (PQ0) and load voltages$\left(V_{Ldq0}\right)$ estimates the reference currents$\left(I_{dq0}\right)$ as below,

$$I_d=\frac{P_1V_{Ld}+Q_LV_{Lq}}{V_{Ld}^2+V_{Lq}^2} \tag{19}$$

$$I_q=\frac{P_1V_{Lq}-Q_LV_{Ld}}{V_{Ld}^2+V_{Lq}^2} \tag{20}$$

$$I_O=\frac{P_{OL}}{V_{OL}} \tag{21}$$

By utilizing Inverse Park Transformation, the acquired reference currents are in rotating reference frame $\left(I_{dq0}\right)$ and transformed into 3ϕform I_{ref_abc}

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix}=\sqrt{\frac{2}{3}}\begin{bmatrix} sin(wt) & cos(wt) & 1 \\ sin\left(wt-\frac{2\pi}{3}\right) & cos\left(wt-\frac{2\pi}{3}\right) & 1 \\ sin\left(wt+\frac{2\pi}{3}\right) & cos\left(wt+\frac{2\pi}{3}\right) & 1 \end{bmatrix}\begin{bmatrix} d \\ q \\ o \end{bmatrix} \tag{22}$$

The feedback loop based hysteresis current controller is used to create shunt converter's switching pulses once real and reference currents are received from measurements. Here, injected currents of shunt converter (I_{sh-abc}) are referred to as the actual currents$(I_{act-abc})$.

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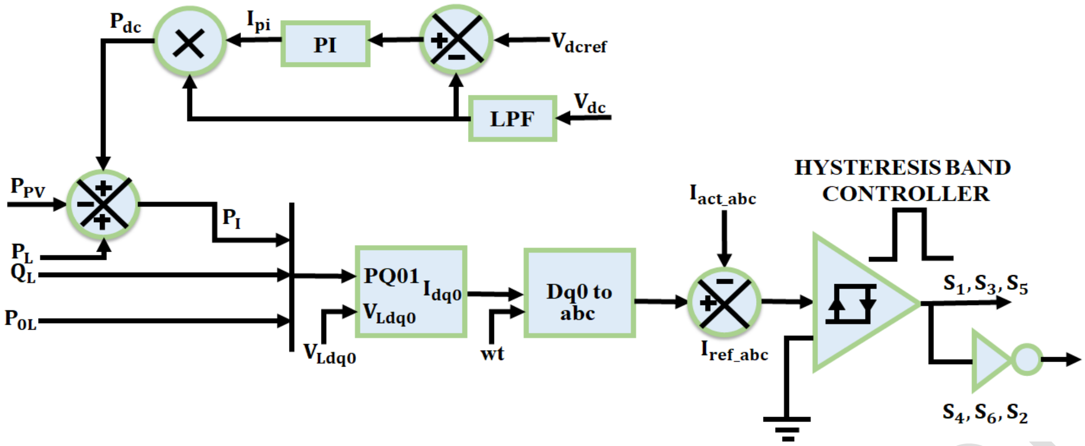

Fig. 8. Shunt converter

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A two-level comparator, hysteresis controller generates switching pulses when limit of current error goes above a predetermined tolerance of hysteresis band (HB_1). By deducting real currents from reference currents, is able to current inaccuracy. Thus, Equations (23, 24) express the switching signal (ON/OFF) of phase "a."

$$\text{If } I_{act\_a} \geq \left(I_{ref\_a} + HB_1\right) \rightarrow S_1 = 0(off), S_4 = 1(on) \tag{23}$$

$$\text{If } I_{act\_a} \leq \left(I_{ref\_a} - HB_1\right) \rightarrow S_1 = 1(on), S_4 = 0(off) \tag{24}$$

Likewise, the switching pulses is estimated for phases 'b' and 'c'.

Series Converter

Voltage swell, sag and interruptions are among the power quality concerns connected to voltage that are lessened by the series converter. Fig. 9 displays the structure for the series converter. It is employed to offset variations in the voltage on source, allowing the load voltages to remain constant despite variations in the load. Furthermore, in order to lessen capacity of shunt converter, series converter share the PV power with it. In order to remove the converter's switching harmonics, an LC filter is attached here. It function as a generator of sinusoidal current and provide a greater impedance channel for load harmonics, preventing the entry of harmonic currents towards the utility grid. Under typical circumstances, series converter supports load's reactive power and compensates for internal voltage drops. In order to sustain power balance on grid side and achieve the necessary load voltage during a sag state, series converter adds voltage in phase with grid voltage. In contrast, to preserve power balance

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under swell conditions, it insert voltage in phase opposition and carry a smaller amount of current than necessary.

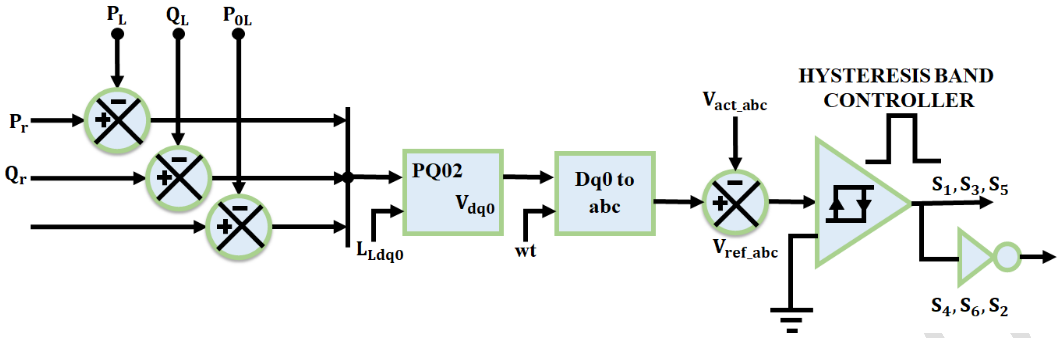

Fig. 9. Series converter

According to Fig. 9, the series converter control system captures sinusoidal voltage reference signal $V_{ref-abc}$ and generates switching pulses to converter. Load powers are taken from Fig. 8 and deducted from reference powers to find power that series converter share. Load and reference powers are determined in section on voltage and power computations. Equations (25) through (27) are used to calculate voltages ($Vdq0$) from assessed load currents (I_{Labc}) and derived powers(PQO_2).

$$V_d = \frac{I_{Ld}\left(P_r - P_L\right) - I_{Lq}\left(Q_r - Q_L\right)}{I_{Ld}^2 + I_{Lq}^2} \tag{25}$$

$$V_q = \frac{I_{Ld}\left(P_r - P_L\right) + I_{Lq}\left(Q_r - Q_L\right)}{I_{Ld}^2 + I_{Lq}^2} \tag{26}$$

$$V_O = \frac{P_{Or} - P_{OL}}{I_{OL}} \tag{27}$$

These voltages are in the $d - q0$ form and uses an inverse park transformation to change to the $a - b - c$ form, where they function as reference voltage signals $(V_{ref-abc})$. For genertaing error signal, measured injected voltage of series converter (V_{se-abc}) is subtracted from the reference voltage signal and considered as an actual voltage. As seen in Fig. 8, hysteresis band controller receives generated error signal. Error signal in hysteresis band controller generates switching pulses for the series converter by comparing it to the higher and lower limits of the hysteresis band (HB_2). A 3 phase 3 leg converter

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makes the series converter contains two switches in each phase. The equations (28)–(29) are used to create switching pulses for phase "a."

$$\text{If } V_{act\_a} \geq \left(V_{ref\_a} + HB_2\right) \rightarrow S_1 = 0\left(off\right), S_4 = 1\left(on\right) \tag{28}$$

$$\text{If } V_{act\_a} \leq \left(V_{ref_a} - HB_2\right) \rightarrow S_1 = 1\left(on\right), S_4 = 0\left(off\right) \tag{29}$$

Likewise, the switching pulses is estimated for phase ‘b’ and ‘c’. Then, the ANN controller is exploited for controlling the function of UAPF.

2-5- ANN Controller

The operations of UAPF is effectively controlled by the integrated ANN controller, is structured as a feedforward neural network comprising three layers such as an input layer, a hidden layer, and an output layer. Input layer receives error current (I_{S-err}), which is the instantaneous deviation between the reference source I_S and actual current. The output layer produces the corresponding duty cycle D_S for controlling the UAPF. Each layer is connected through neurons (nodes), which apply weighted transformations and activation function to propagate signals forward. The hidden layer comprises of 10 neurons, each employing the sigmoid activation function for introducing non-linearity and enhances learning capabilities. The output layer utilizes a linear activation function to provide a continuous control signal suitable for PWM generation.

The ANN controller operates in two distinct phases: training and testing. During training, a supervised learning approach is adopted using a dataset generated from simulated UAPF operation under varying load conditions. Training process utilizes Mean Squared Error (MSE) as the loss function and is optimized using propagation algorithm with learning rate of 0.01. Model is trained until convergence is attained with minimal error between predicted and actual duty cycles.

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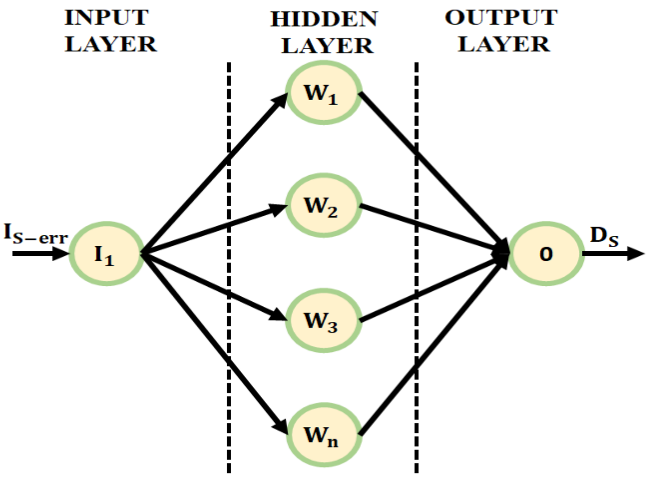

Fig. 10. Structure of ANN controller

Fig.10. displays the structural design of the ANN controller operates in real-time to regulate the UAPF be generating appropriate PWM pulses, thereby ensuring effective compensation and maintains power quality.

3. Results and Discussion

This research examines various issues, including power factor, source current, and load voltage. The developed work is implemented at MATLAB/Simulink and comparison analysis is made with conventional approaches. Table 1 represents the specification of parameters for a developed work.

Table 1. Specification of Parameters

Parameter	Specification
AC Source	
Load Resistance	100Ω
Load Inductance	10mH
PV system	
Voltage (Open circuit)	22.6V
Voltage (Short circuit)	12V
Switched inductor based Boost-Luo converter	
L_i	$4.7\ mH$
L_{a1}, L_{a2}	$1mH$
C_{a1}	$22\ \mu F$
C_0	$2200\mu F$
Switching Frequency	10 kHz

Case 1: Step Magnitude (-0.4)

In this case, the efficacy of developed work is analyzed in the voltage sag condition.

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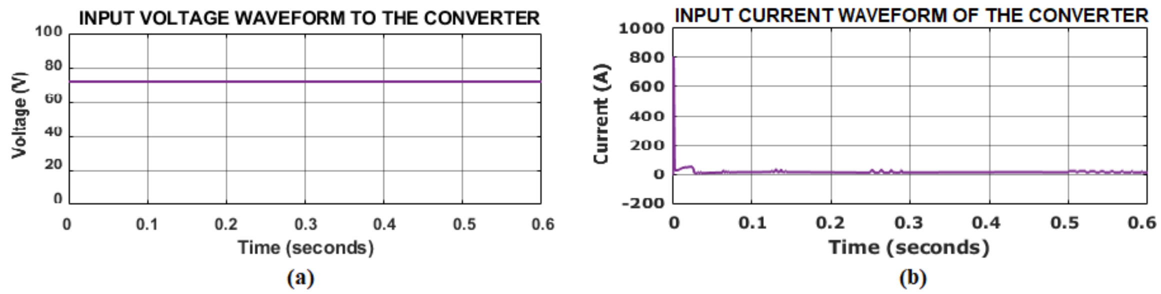

Fig. 11. Input waveform of converter

Fig. 11 (a) and (b) represents input waveform of converter for voltage and current. Input voltage of converter is continued at constant value of $72\ V$ during system. Also, input current is changed in starting time and is settled constant value of $36\ A$ with small fluctuations.

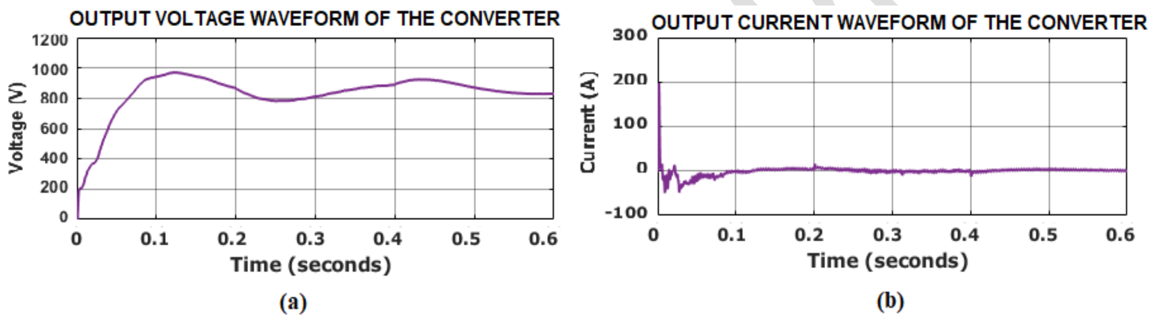

Fig. 12. Output waveform of converter

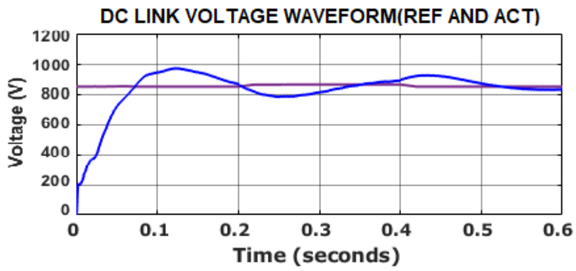

Fig. 13. Waveform of DC link voltage

The waveform for output of converter for voltage and current is specified in Fig. 12(a) and (b). At first, converter's output voltage is varied and is finally sustained stable value of $815\ V$. Similarly, converter's output current is changed in initial period and maintained a value of $3\ A$. Fig. 13 reveals the waveform of DC link voltage, which is initially varied and sustained a stable value of $840\ V$.

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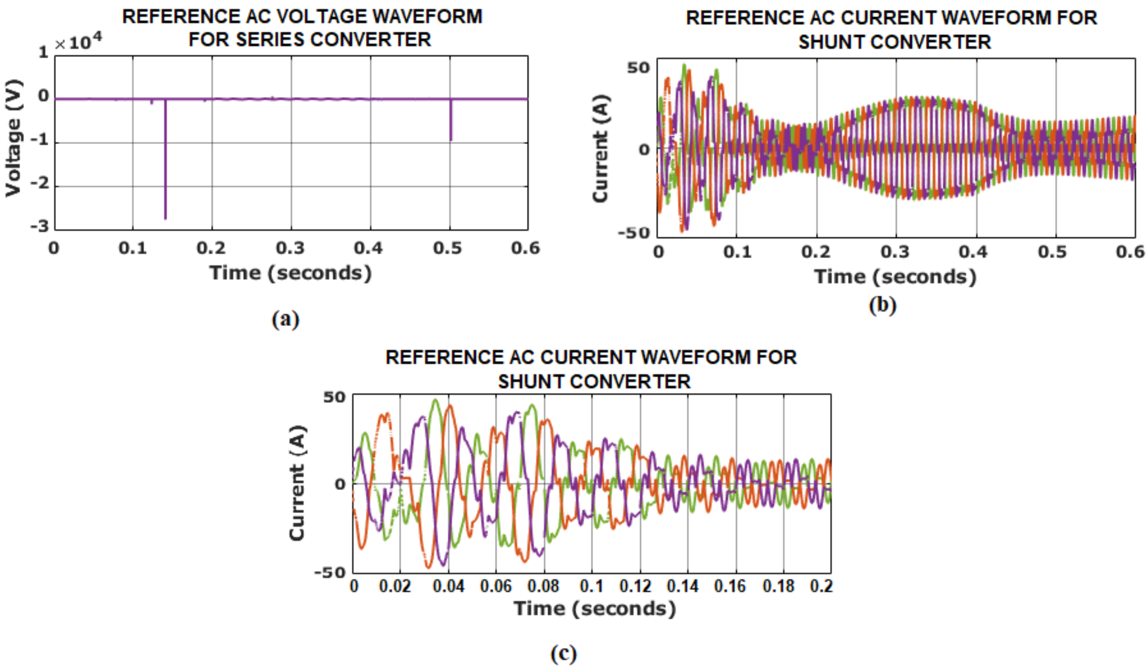

Fig. 14. Waveform of UAPF

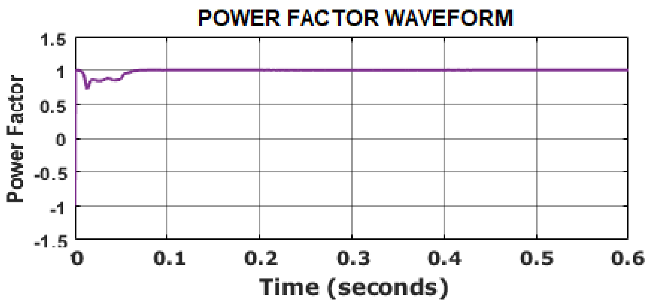

Fig. 15. Waveform of power factor

The reference AC voltage and current waveform of series and shunt converter is displayed in Fig. 14 (a) and (b). The series converter's reference AC voltage sustained a stable value of $1000V$ with small fluctuations. The shunt converter's reference AC current maintained a stable value with little distortions between $0.2\ to\ 0.4\ s$. Fig. 14 (c) shows the zoomed view of reference AC current waveform of shunt converter and is sustained at a stable value of $15\ A$ (after $0.13\ s$). The waveform of power factor is represented in Fig. 15. PF value is varied in starting period and is sustained a stable value of 0.98 throughout the system.

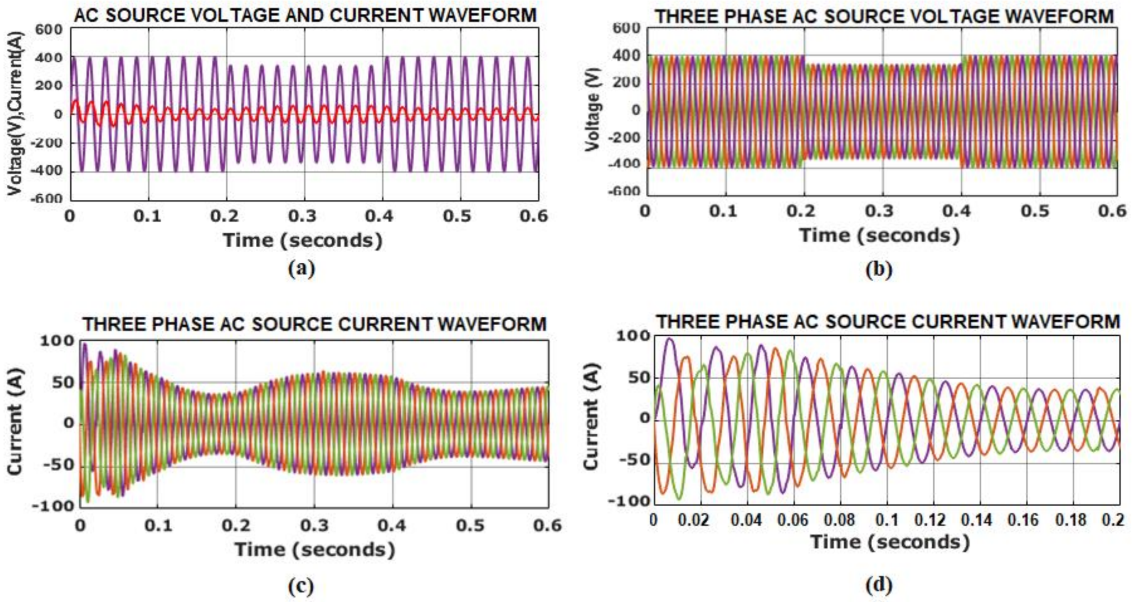

Fig. 16. Waveform of source side with -0.4 step magnitude

The combination of AC source voltage and current is sustained at a stable value of $310V$, (from $0.2\ to\ 0.4\ s$) as shown in Fig. 16 (a). Sag magnitude of $-0.4\ p.u$ is presented in time period ranging from 0.2 to 0.4 s. Voltage supply except effect of any power quality problem is of magnitude $400V$. Nevertheless, over presence of -0.4 p.u voltage sag, voltage is diminishes from $400\ to\ 370V$ since $0.2s$ as indicated in Fig. 16 (b). Source current is seen in Fig. 16(c) and is maintained a stable value with small variations (from $0.2\ to\ 0.4\ s$). Fig. 16 (d) reveals the zoomed view of source current and is varied in initial period and finally, it sustained a stable value.

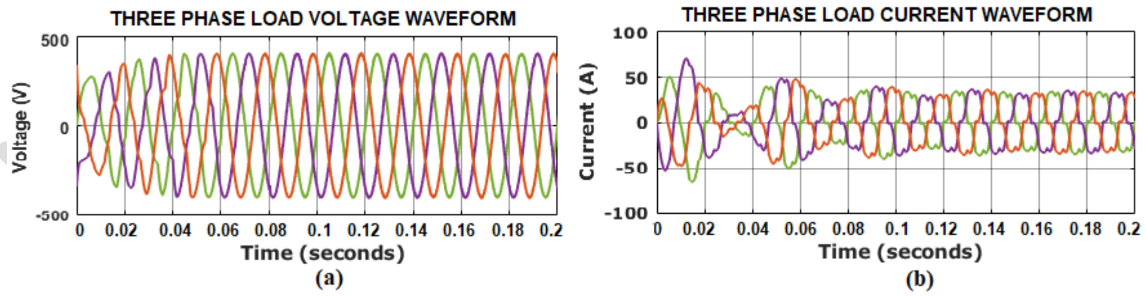

Fig. 17. Waveform of load side

Waveform of load side for voltage and current is displayed in Fig. 17 (a) and (b). Voltage on load have no changes (small spike) ever there is a voltage sag issues in the voltage at source side. The load current is changed in initial period and is settled a stable value throughout the system.

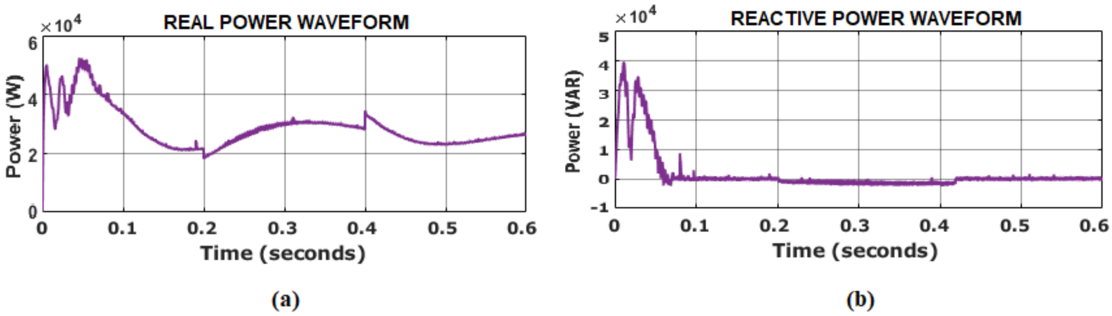

Fig. 18. Waveform of power

Fig. 18 (a) and (b) portrays the waveform of real and reactive power which demonstrates active management of reactive power and compensation to manage varying load conditions. The real power is maximum and is received from the grid and the reactive power is nearly 0.

Case 2: Step magnitude (+0.4)

In this case, PQ problem of voltage swell (+0.4) and performance of UAPF is examined.

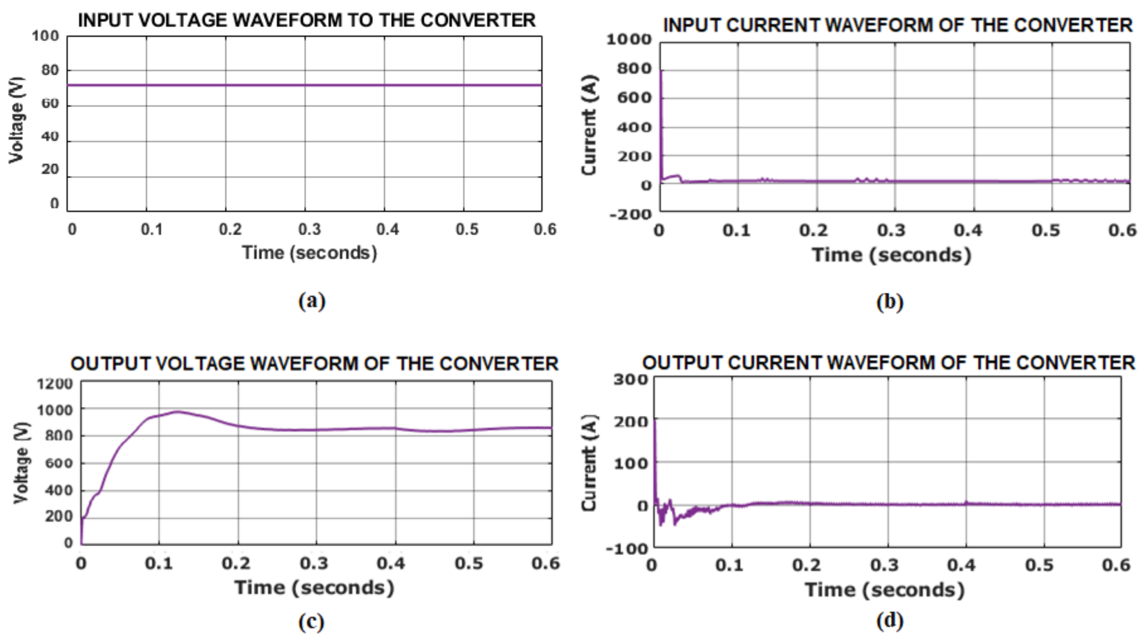

Fig. 19. Waveform of converter

Input waveform of converter for voltage and current is represented in Fig. 19 (a) and (b). Input voltage value of converter is maintained a stable value of 72 V during system. Converter's input current is varied in initial time and finally it is settled a constant value of 10 A. Fig. 19 (c) and (d) illustrates the

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waveform for output voltage and current of converter. Converter's output voltage is initially varied and maintained at $820\,V$ throughout system. At first, converter's output current is fluctuating and it continued stable value of $10\,A$.

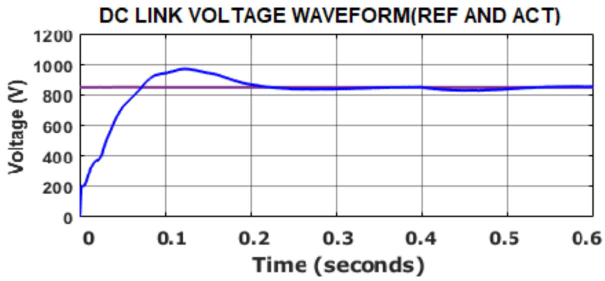

Fig. 20. Waveform of DC link voltage

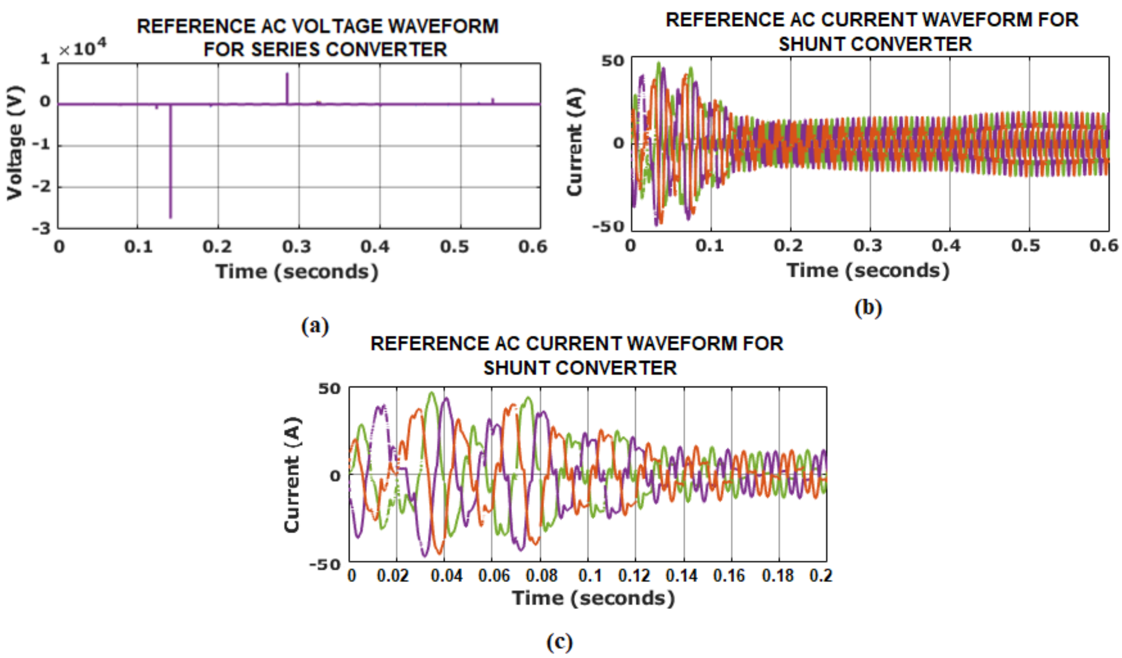

Fig. 21. Waveform of UAPF

Value of DC link voltage is varies in starting period and settled at a constant value of $820\,V$ as presented in Fig. 20. The reference AC voltage and current waveform of series and shunt converter is indicated in Fig. 21 (a) and (b). Reference voltage of series converter sustained a value of $1000\,A$ with small fluctuations. The shunt converter's current value is changed in starting time and is settled a stable value. Also, the zoomed view of waveform for shunt converter is represented in Fig. 21 (c).

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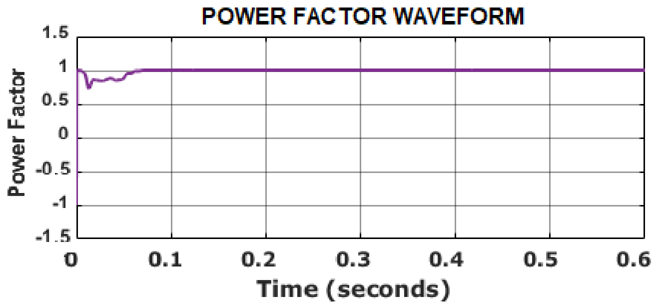

Fig. 22. Waveform of power factor

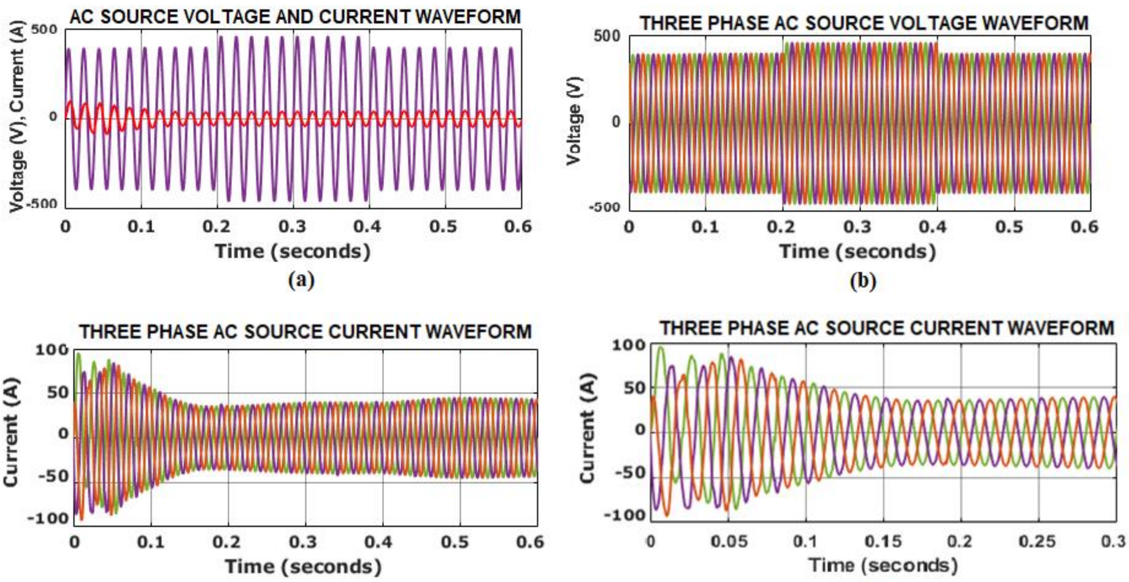

Fig. 23. Waveform of source side with 0.4 step magnitude

Fig. 22 indicates the waveform of power factor, which is varied in starting period and settled to the nearest value of 1. The combined source voltage and current waveform is increased in between $0.2\ to\ 0.4\ s$, which is revealed in Fig. 23 (a). Fig. 23 (b) displays the waveform of source voltage (voltage swell condition), which is improved from $400\ to\ 470\ V$ during the interval of $0.2\ to\ 0.4\ s$. The source current waveform initially changed and is settled a constant value as depicted in Fig. 23 (c). Zoomed view of source current waveform is revealed in Fig. 23 (d).

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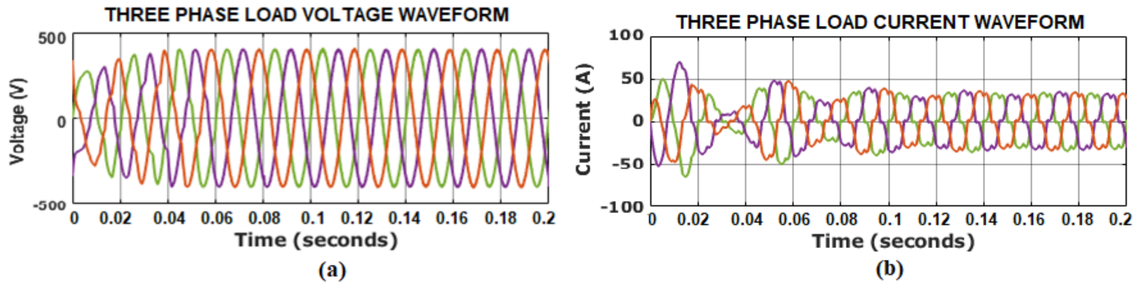

Fig. 24. Waveform of load side

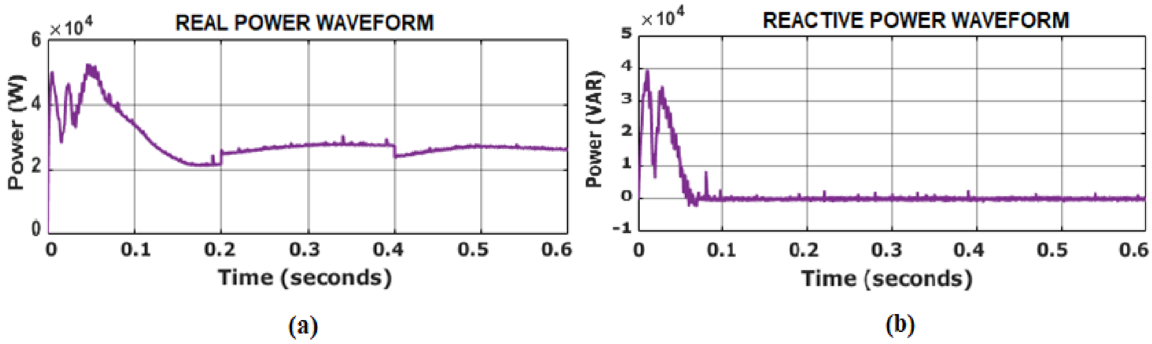

Fig. 25. Waveform of power

Fig. 24 (a) and (b) represents waveform of load voltage and current. At first, the value of load voltage is changed and is maintained a stable value of $400\ V$. Also, load voltage is varied in starting time and is sustained a value of $35\ A$ with small distortions. Real and reactive power's waveform is illustrated in Fig. 25 (a) and (b). Real power is improved and reactive power is low in voltage swell condition.

Case 3: LOAD CHANGES

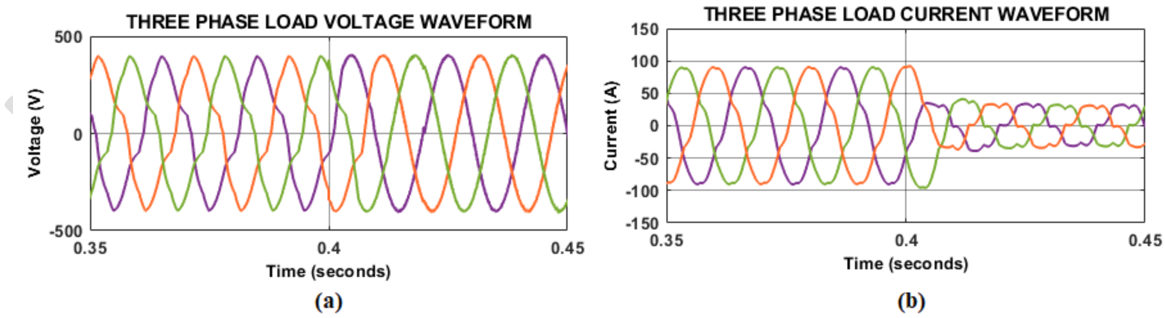

Fig. 26. Waveform of three-phase load.

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Fig. 26. Presents the waveform of three-phase load under case 3: load changes. Fig. 26(a) shows three-phase voltage waveform of load during dynamic change in the load. The three voltage profiles of all three phases are sinusoidal and balanced, demonstrating that the series converter in UAPF maintains voltage stability even under sudden changes in load conditions. Fig. 26(b) displays waveform of three-phase load current, which is initially sinusoidal in nature but becomes distorted at around 0.42 seconds, coinciding with a load change. This distortion indicates the nonlinearity introduced through the load change. The shunt converter controlled by ANN reacts by compensating the harmonics in the current and re-establishing waveform symmetry, thus maintaining power quality.

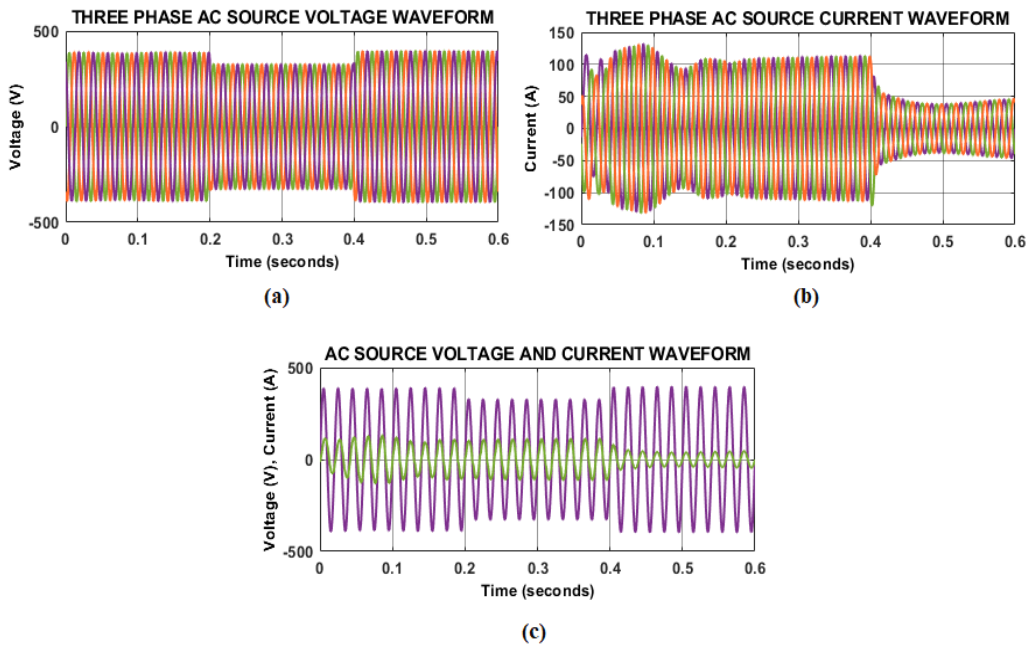

Fig. 27. Waveform of AC source.

Fig. 26. represents the three-phase ac source waveform under load changing scenario. Fig. 26(a) shows the AC source voltage waveform of the three-phase AC source during dynamic load change. All three phases have a balanced sinusoidal pattern with steady amplitude and frequency throughout period, indicating voltage stability is achieved along with prevention of power quality degradation. Fig. 26(b) shows the three-phase AC source current waveform, which is initially sinusoidal but contains small deviations in amplitude and phase timing. These deviations are due to how the system responds to sudden changes in loads. Fig. 26(c) indicates the combined AC source voltage and current waveform,

with a focus on voltage and current phase relationship. The waveform provides evidence of near-synchronous alignment, which implies enhanced PF and lower reactive power flow. This proves performance efficacy of ANN controller and UAPF in ensuring system efficiency during load disturbance.

Case 4: PV CUT OFF

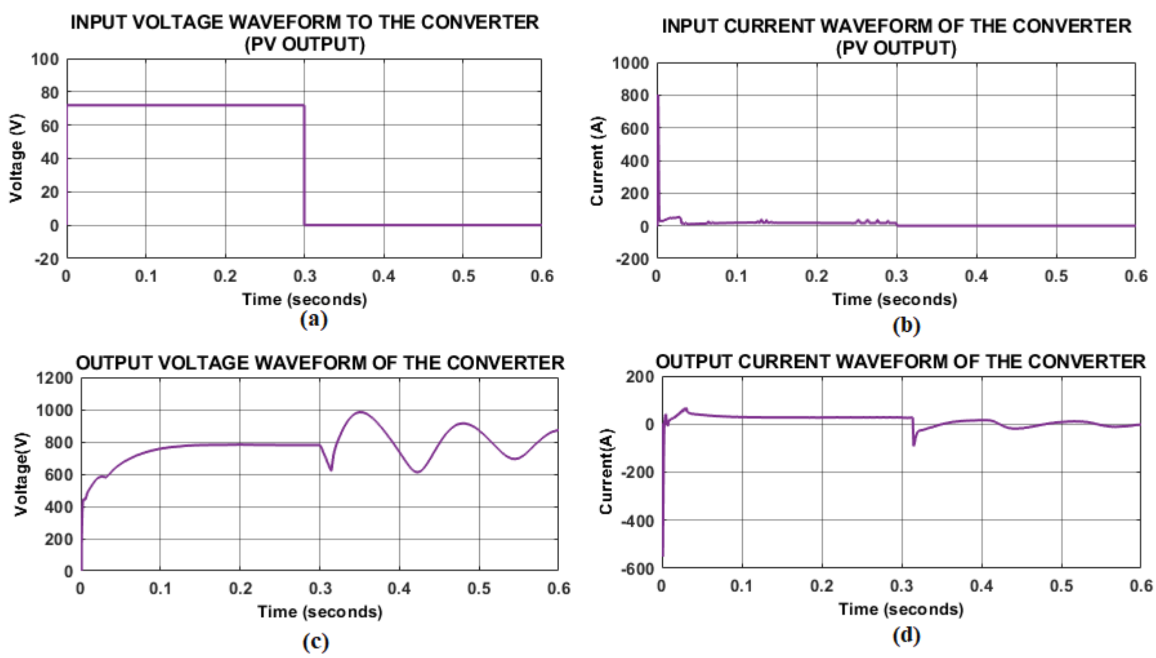

Fig. 28. Waveform of PV system.

Fig. 28. displays converter input and output waveforms under PV cut off condition, in fig. 28 (a) converter input PV output voltage is constant at about 70V until 0.3 seconds when it suddenly falls to 0V, representing a total cut-off of the PV source. Fig. 28 (b) illustrates the input current wave to the converter. The current is peaks at around 800A before it drops to 0 A suddenly at 0.3 seconds, verifying the PV source has stopped providing power. Fig. 28 (c) displays output voltage waveform of the converter that starts oscillating noticeably after 0.3 seconds. Oscillations reflect the converter's effort to regulate output voltage utilizing stored energy in passive elements. Fig. 28 (d) indicates the converter output current waveform, which fallen steeply at 0.3 seconds and, thereafter, recovers with oscillations. This trend is indicative of the converter's response to transient shutdown of PV, the proposed controller

strive to maintain current supply to the load by the use of grid support as well as compensation within the system.

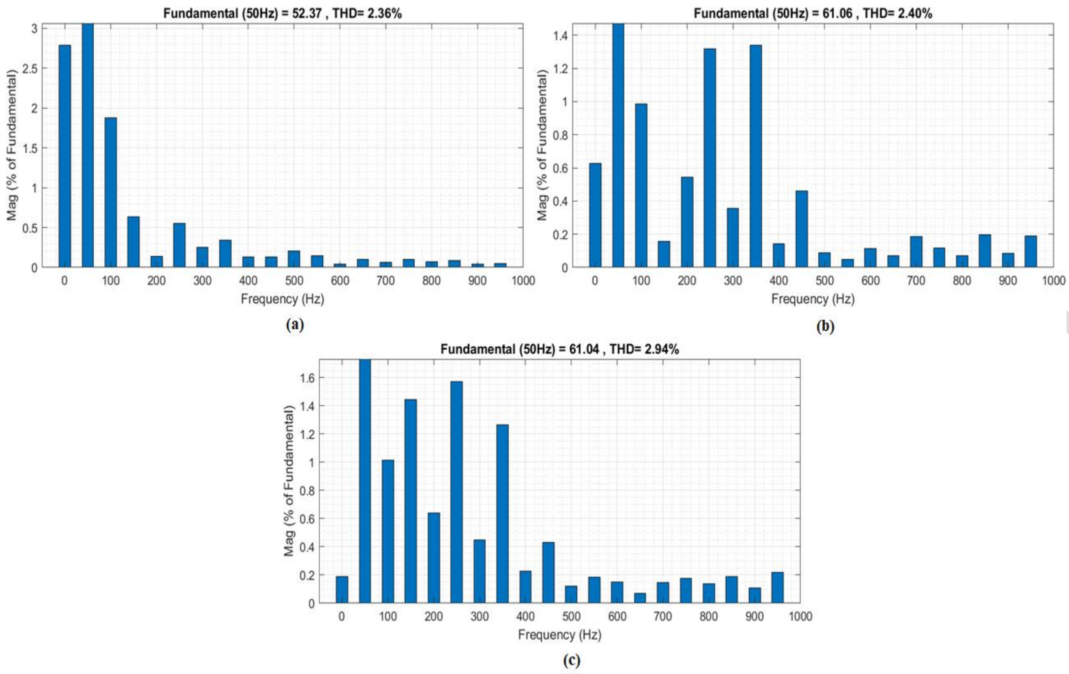

Fig. 29. Waveform of THD

The three phase waveform of Total Harmonic Distortion (THD) is denoted in Fig. 29 (a), (b) and (c). The developed work attained the lower THD, which is lesser than 5 %.

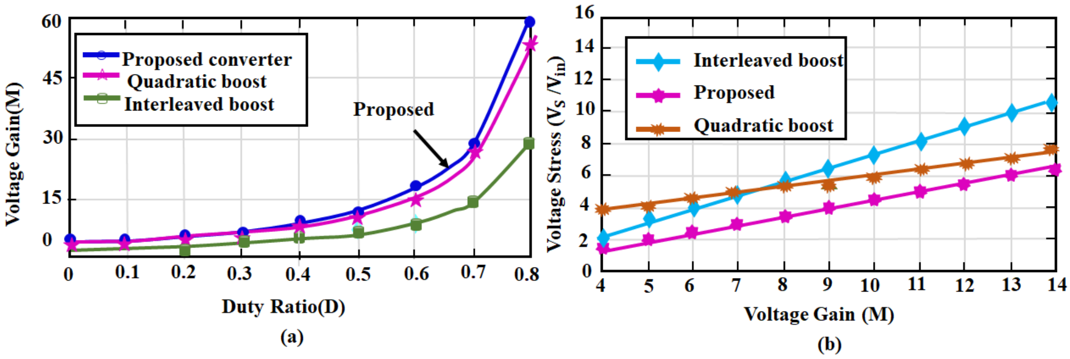

Fig. 30. Voltage gain and stress comparison

The comparison of voltage gain for Quadratic boost [22], interleaved boost [23] and developed converter is illustrated in Fig. 30 (a). From that, the developed converter attains the greater voltage gain than other converters. Also, developed converter have reduced voltage stress than Quadratic boost [22], interleaved boost [23] converter as represented in Fig. 30 (b). The comparison with other converters in

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terms of component counts, voltage gain and efficiency is revealed in Table 2. The Quadratic boost [22], interleaved boost [23] and Transformerless quadratic boost converter [24] have the highest number of components than the developed converter.

Table 2. Comparison with other converters

Reference	Number of switch	Number of inductors	Number of diodes	Number of capacitors	Voltage gain	Efficiency
[22]	1	1+1 coupled inductor	5	3	$\frac{(3-D)}{(1-D)^2}$	93.2%
[23]	6	6	14	8	$\frac{1}{1-D}$	91.5%
[24]	1	3	5	3	$\frac{2}{(1-D)^2}$	94.1%
Proposed	1	3	5	2	$\frac{4-D}{1-D}$	94.32%

Table 3. Comparison of power factor for voltage sag

Voltage Sag				
		Phase A	**Phase B**	**Phase C**
PV-BESS-UPQC [25]	**Grid voltage**	0.913	0.913	0.905
	Grid voltage	0.921	0.924	0.924
	Load voltage	0.956	0.949	0.948
	Load current	0.963	0.963	0.962
PV-DG-DSTATCOM [28]	**Grid voltage**	0.912	0.910	0.908
	Grid voltage	0.918	0.920	0.919
	Load voltage	0.951	0.947	0.945
	Load current	0.958	0.9860	0.957
PV-UPQC [29]	**Grid voltage**	0.914	0.916	0.913
	Grid voltage	0.922	0.925	0.924
	Load voltage	0.961	0.958	0.957
	Load current	0.965	0.968	0.966
Proposed	**Grid voltage**	0.989	0.996	0.993

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	Grid voltage	0.988	0.989	0.988
	Load voltage	0.992	0.995	0.992
	Load current	0.983	0.994	0.988

Table 4. Comparison of power factor for voltage swell

Voltage Swell				
		Phase A	**Phase B**	**Phase C**
PV-BESS-UPQC [25]	**Grid voltage**	0.942	0.943	0.945
	Grid voltage	0.957	0.956	0.956
	Load voltage	0.978	0.976	0.975
	Load current	0.973	0.972	0.972
PV-DG-DSTATCOM [28]	**Grid voltage**	0.938	0.940	0.939
	Grid voltage	0.948	0.947	0.949
	Load voltage	0.973	0.970	0.969
	Load current	0.968	0.970	0.969
PV-UPQC [29]	**Grid voltage**	0.944	0.946	0.945
	Grid voltage	0.955	0.954	0.956
	Load voltage	0.981	0.979	0.978
	Load current	0.976	0.978	0.977
Proposed	**Grid voltage**	0.981	0.986	0.995
	Grid voltage	0.985	0.984	0.997
	Load voltage	0.993	0.987	0.990
	Load current	0.989	0.995	0.993

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The comparison of power factor for voltage sag and swell is represented in Table 4 and 5. The proposed PV based UAPF attains the better power factor for all phases than the PV–Battery Energy Storage System–Unified Power Quality Conditioner (PV-BESS-UPQC) [25], PV Distributed Generation (DG) and Distribution Static Synchronous Compensator (DSTATCOM) (PV-DG-DSTATCOM) [26] and PV-UPQC [27] approach.

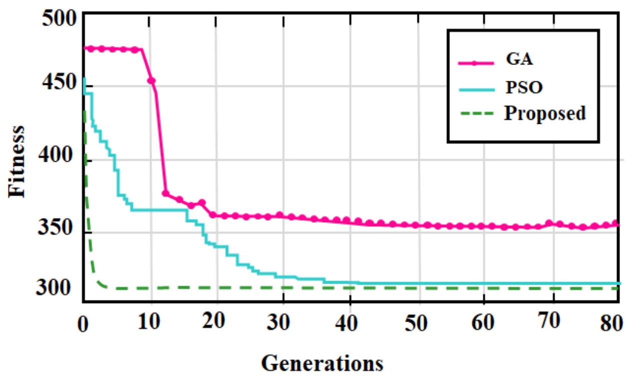

Fig.31 Comparison of convergence speed.

Fig.31 presents the convergence behaviour of optimization algorithms such as Genetic Algorithm (GA) [28], Particle Swarm Optimization (PSO) [29] and proposed MRKO approach over 80 generations. The proposed MRKO algorithm achieves superior convergence behaviour, demonstrating significantly lower objective value within fewer generations and sustains consistently throughout the system.

4. Conclusion

In order to improve power quality, this study proposes a PV-powered unified active power filter with an intelligent ANN controller. By using boost-luo converter with switched inductor increases low voltage from PV system. Stabilized voltage is reached and PI controller parameters are effectively tuned by using MRKO algorithm based PI controller. The utilization of UAPF permits the compensation of harmonics produced by non-linear loads, voltage sag and swell, and other voltage disturbances. For controlling the operation of UAPF the ANN controller is exploited, which is essential for maintaining the voltage levels within the desired range. The developed work is applied in MATLAB/Simulink and comparative analysis is made with conventional approaches. The comparative outcomes reveal that the developed approach, which outperforms the other standard methodologies, is a good option for refining the PQ of grid-connected PV systems. The outputs prove that the developed approach delivers THD lesser than 5%, which is highly optimum in improving the PQ of the entire system.

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