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A New High Step-down Converter with Low Ripple Current and High Efficiency

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ABSTRACT: This paper introduces a new high step-down converter that achieves zero voltage switching in both primary and auxiliary switches without relying on coupled inductors, thus ensuring low ripple in input and output currents. The auxiliary circuit is optimized with the fewest possible components, facilitating zero voltage switching for the main and auxiliary switches and solving the reverse recovery issue of freewheeling diodes through zero current switching conditions. Additionally, this design reduces voltage stress on the switches, allowing the use of MOSFETs with lower drain-source resistance. A key advantage of this converter is that it avoids using coupled inductors, which eliminates issues related to leakage inductance and potential increases in the converter's size and weight. This enhances the converter's efficiency and practicality. The auxiliary circuit design can also be extended to multiple phases, making it adaptable for various applications. The control mechanism is simple because the auxiliary switch operates in complementary with the main switch, simplifying the overall circuit design and integration. The proposed converter's design and operational principles have been validated through PSpice simulations, and a 90W prototype has been constructed. Experimental results demonstrate an impressive 95 percent efficiency at full load.

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1- Introduction

Due to the recent advancements in computing and telecommunications, there has been a rapid increase in the deployment of information and communication technology (ICT) equipment, driven by demands for greater compactness, efficiency, and higher power density [1-3]. Moreover, these systems are supplied power from the electrical grid through isolated converters that are highly efficient. For ICT equipment, non-isolated converter architectures are often preferred over isolated ones due to their reduced number of components, simpler design, and control mechanisms. A conventional buck converter consists of one switch, one diode, and two passive elements: an inductor and a capacitor. However, this configuration is challenged by high voltage stress on its switching elements, leading to significant conduction and switching losses [5]. Additionally, the efficiency of the converter is compromised in high step-down scenarios due to operating at low-duty cycles, which intensifies the current stress on the devices [6,7]. Various strategies have been proposed to address these issues in high step-down applications [8-11], including the use of coupled inductors (CIs) and series capacitor techniques, or employing cascading structures.

The method of changing the turn ratio of coupled inductors (CIs) to achieve high step-down ratios is discussed in [9,10]. This approach makes minimal changes to the traditional buck converter design. However, it faces several problems: it requires a circuit to handle leakage inductance energy, which causes voltage spikes and complex control; the voltage stress on switches remains high, leading to greater switching losses and lower efficiency; and it needs a larger core size because of the significant DC magnetizing inductance current. References [11-13] introduce a clamping capacitor to the primary winding of the coupled inductor, aiming for better step-down ratios and reduced DC magnetizing inductance current. Despite these improvements, issues such as large DC magnetizing currents and fluctuating output currents persist, making CI-based converters less appealing for ICT equipment applications. One innovative strategy involves cascading converters, a technique referenced in [9]. Despite the quadratic dependency of the voltage ratio on the duty cycle, this method is complicated by the increased number of components and a complex control circuit. Efforts to reduce the number of switches by merging series converters into a single structure were made in [11,12], though this led to higher voltage and current stress, escalating both switching and conduction losses.

The use of a coupled inductor to enhance the duty cycle presents another viable solution. It introduces an additional degree of freedom to the system and facilitates

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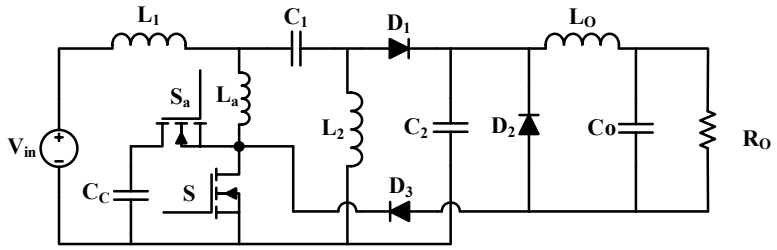

Fig. 1. Schematic view of the proposed high step-down converter

the development of soft-switching capabilities. Techniques applying this principle, as seen in [13] through [17], feature a low voltage ratio but suffer from a high component count. Additionally, converters mentioned in [15,16] are criticized for their pulsating output current. Issues with load protection arise in cases where the switch is compromised, as noted in [17] and [18]. The inclusion of a coupled inductor in the output, results in a pulsating current, with the energy stored in leakage inductance causing voltage spikes across the switch. To mitigate these spikes, a passive clamp circuit was introduced in [19], and an active clamp circuit was adopted in [20] to ensure soft-switching conditions, albeit at the expense of an increased semiconductor device count.

Another way to extend the duty cycle is by using a large capacitor in the power delivery path, known as the series capacitor technique. In this method, the capacitor charges and discharges during the freewheeling mode, ensuring automatic current balance across different phases. This technique, combined with a coupled inductor, was introduced in [21]. However, it requires four semiconductor elements, making it costly, and the circuit still suffers from pulsating output current.

This paper describes a novel high step-down converter design. It achieves zero voltage switching for both the main and auxiliary switches. Unlike conventional designs, it avoids using coupled inductors, resulting in minimal input and output current ripple. The auxiliary circuit is cleverly designed with minimal elements. This allows for zero voltage switching conditions and eliminates the issue of reverse recovery current in the freewheeling diodes by Zero current condition.

2- Proposed high step-down converter

Fig. 1 showcases the design of the suggested high step-down converter. This converter is made up of three inductors: the input inductor L_1, the output inductor L_o, and the interface inductor L_2. These inductors are excluded from the analysis because their current ripple is significantly large. Furthermore, it includes capacitors C_1, C_2, and C_o, which serve as energy storage components with substantial values, and their voltage is assumed to be steady throughout a cycle. The converter is equipped with four diodes, D_1 through D_4, along with a primary switch S and a secondary switch S_a. Additionally, the converter features a clamp capacitor C_C and an auxiliary inductor L_a, which aids in achieving Zero-Voltage (ZV) conditions.

2- 1- Converter operation

Fig. 2 presents the switching waveforms for the converter across a single switching cycle, revealing that the converter operates through six distinct modes within this period. The capacitors, C_1, C_2, C_C, and C_o, are characterized by their high values, leading to a constant voltage throughout the cycle. Conversely, the presence of input and output inductors, L_1

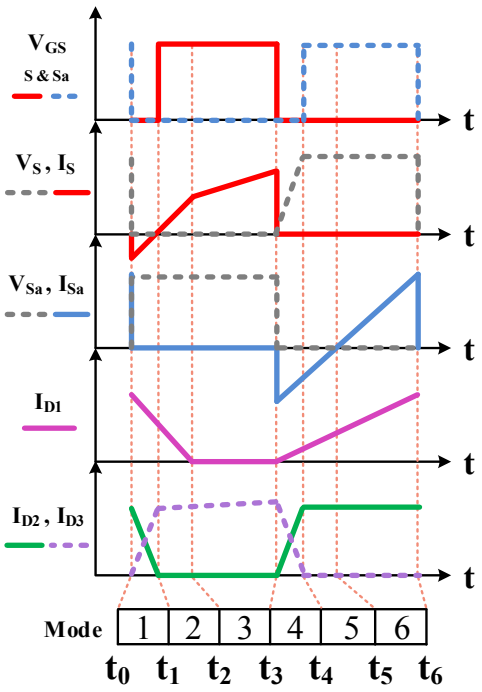

Fig. 2. Switching waveforms of the proposed step-down converter

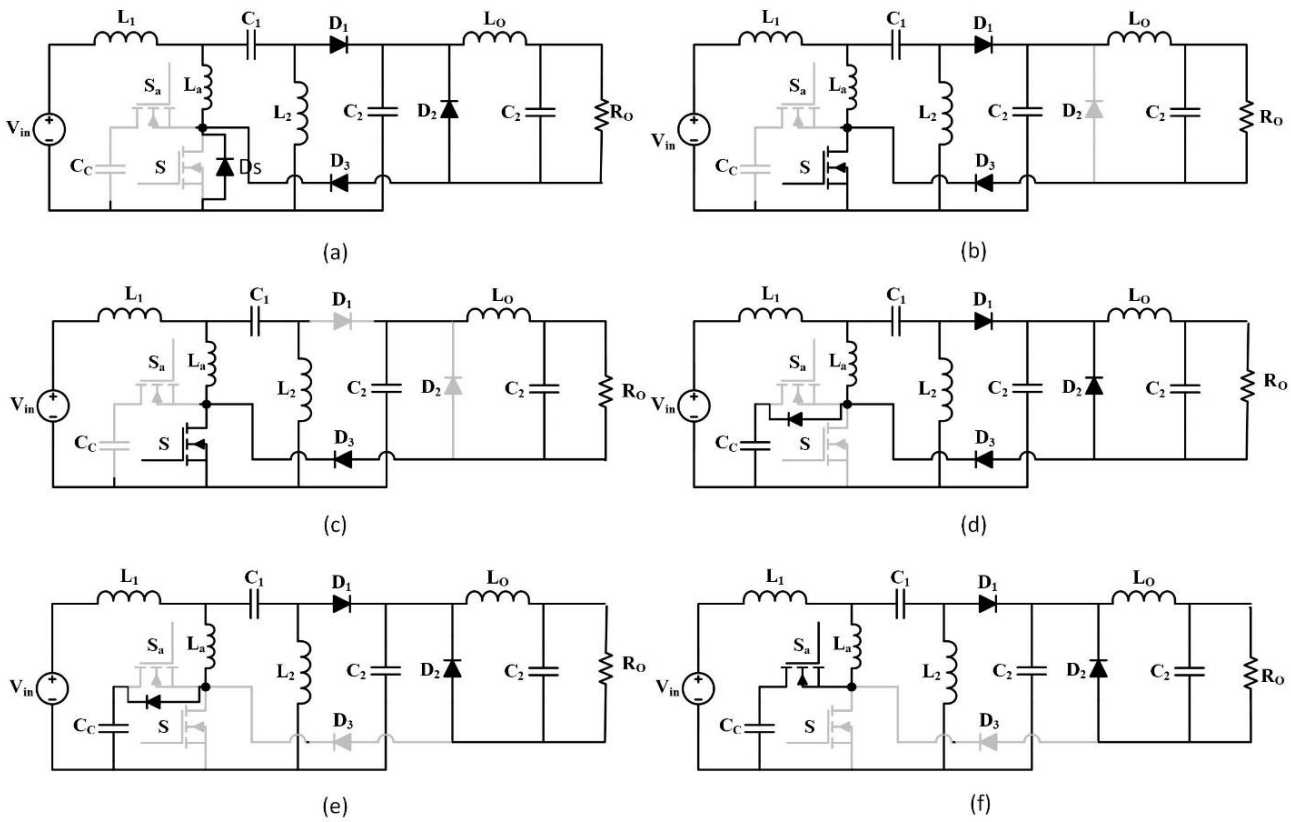

Fig. 3. The equivalent circuit in each mode of the proposed converter (a) first mode (b) second mode (c) third mode (d) fourth mode (e) fifth mode (f) sixth mode

and L_o, ensures that the current ripple at both the input and output stages remains minimal. Both the main switch and the auxiliary switch operate at the same frequency, with their activation occurring in a complementary manner. Fig. 3 displays the equivalent circuit diagrams of the converter in each mode. Prior to entering the first mode, the main switch S is turned off while the auxiliary switch S_a is on, and diodes D_1 and D_2 are active, allowing the output inductor L_o to discharge through the load.

The first mode: The first mode begins when S_a is turned off, and inductor L_a discharges capacitor S_1 and capacitor S_2 to turn on S_1 body diode. In this mode, the current is transferred from diode D_2 to diode D_3.

The second mode: When S_1 body diode is turned on, S_1 can be turned on under ZV conditions. In this mode, D_1 current is decreased linearly until it will be turned off under ZC conditions. This mode ends when S_1 current reaches I_{L1} current.

The third mode: This mode starts when D_1 is turned off. In this mode, L_1 starts being charged linearly with the slope of $\frac{V_{in}}{L_1}$ and inductor L_2 is also charged with the slope of $\frac{V_{C1}}{L_2}$. In addition, L_o is charged with a slope of $\frac{V_{C1}-V_o}{L_o}$.

The fourth mode: This mode starts when S is turned off. In this mode, inductor L_a charges capacitor S_1 and discharges capacitor S_2, so that its body diode is turned on. In this mode, diodes D_2 and D_3 are turned on and off respectively.

The fifth mode: S_a body diode is on and from this moment S_a can be turned on under ZV conditions. In this mode, the current is increased linearly with the slope of $\frac{V_{Cc}-V_{C1}}{L_a}$. This mode ends when the current is transferred from S_a body diode to S_a.

The sixth mode: In this mode, S_a is on and inductor L_o is being discharged at the output. In addition, L_1 is also discharged with the slope of $\frac{V_{in}-V_{Cc}}{L_1}$ and capacitors C_1 and C_2 will be charged. This mode ends when S is turned on again.

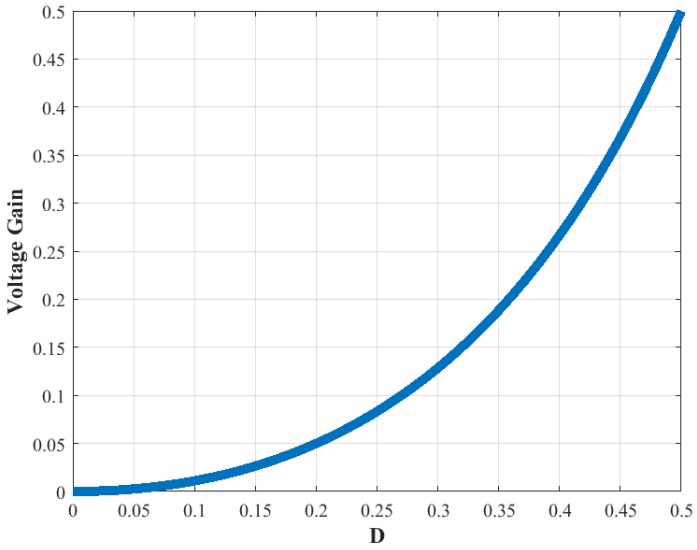

Fig. 4. Proposed converter gain in terms of duty cycle changes

3- Analysis of step-down buck converter

This section will analyze the suggested converter, focusing on its voltage gain, voltage stress across components, current through its elements, and the design of these elements. The methodology behind the converter's design will also be detailed. This exploration aims to illuminate the operational capabilities of the converter, especially its efficiency in voltage conversion and how it handles the electrical stress on its components. The considerations behind selecting specific component values and arrangements to enhance performance and longevity will be discussed. By concluding this section, readers will gain insight into the converter's voltage gain achievements and the strategies implemented to ensure component reliability and circuit efficiency under varying operational conditions.

3- 1- converter gain

By writing the volt-second balance on inductors L_1, L_o, and L_2, the voltage of capacitors C_1, C_2, and C_o will be obtained, and with their help, the converter gain in CCM mode will be obtained. Fig. 4 demonstrates the proposed converter gain in terms of duty cycle changes.

$$V_i DT + (V_i - V_{C1} - V_{C2})(1-D)T = 0 \tag{1}$$

$$V_{C1} DT - V_{C2}(1-D)T = 0 \tag{2}$$

$$(V_{C2} - V_O)DT - V_O(1-D)T = 0 \tag{3}$$

$$V_{C1} = \frac{V_i - V_{C2}(1-D)}{1-D} \tag{4}$$

$$V_{C2} = \frac{D}{1-D} V_{in} \tag{5}$$

$$M = \frac{V_O}{V_{in}} = \frac{D^2}{1-D} \tag{6}$$

In DCM (Discontinuous Conduction Mode), the input current becomes discrete. In this mode, the converter's power depends on the maximum input voltage, load, and duty cycle. Considering the permissible ripple and the relationship of the input current in DCM, the converter's gain can be calculated in this mode.

$$I_{in} = \frac{1}{2} D(D + D')T^2 \frac{V_{in}}{L_1} \tag{7}$$

$$L_{eq} = \frac{TD^2 V_{in}^2}{4P_{in}} \tag{8}$$

$$L_{eq} = \frac{L_1 L_2}{L_1 + L_2} \tag{9}$$

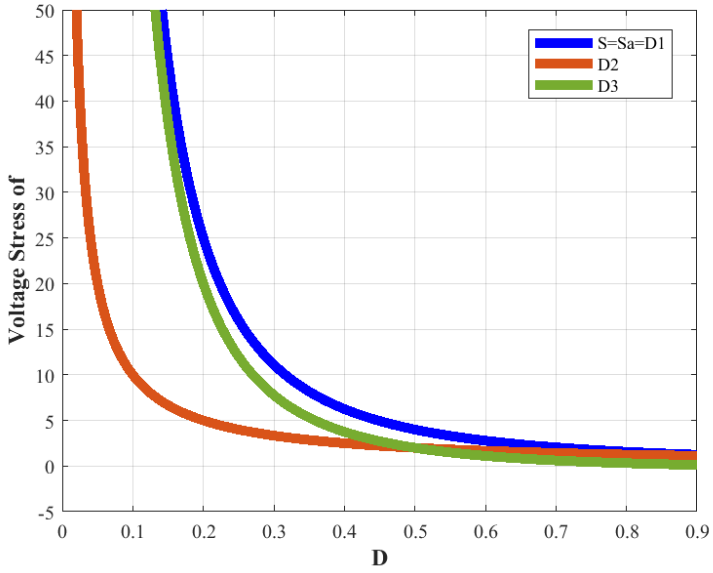

Fig. 5. Normalized stress diagram of the semiconductor elements of the proposed high step-down converter in terms of duty cycle changes

$$M_{DCM} = \sqrt{\frac{4L_{eq}f}{RD^2}} \tag{10}$$

3- 2- Voltage stress of switches

To calculate the element's voltage stress, it is enough to write KVL in the path of the element when that element is off. So:

$$V_S = V_{Sa} = \frac{V_{in}}{1-D} = \frac{V_O}{D^2} \tag{11}$$

$$V_{D1} = \frac{V_O}{D^2} = \frac{V_{in}}{1-D} \tag{12}$$

$$V_{D2} = \frac{V_O}{D} = \frac{V_{in}D}{1-D} \tag{13}$$

$$V_{D3} = V_{in} \tag{14}$$

Fig. 5 demonstrates the normalized stress diagram of the semiconductor elements of the proposed high step-down converter in terms of duty cycle changes.

3- 3- Design of converter passive elements

To calculate the size of L_1, L_2, and L_o, it is sufficient to use the inductor basic equation.

$$L_1 = \frac{DV_{in}}{f\,\Delta I_{L1}} \tag{15}$$

$$L_2 = \frac{DV_{in}}{f\,\Delta I_{L2}} \tag{16}$$

$$L_O = \frac{V_{in}D^2}{f\,\Delta I_O} \tag{17}$$

In addition, the equation between capacitors can be used to calculate capacitors C_1, C_2, and Co.

$$C_1 = \frac{D^2 I_O}{f\,\Delta V_{C1}} \tag{18}$$

$$C_2 = \frac{DI_O}{f\,\Delta V_{C2}} \tag{19}$$

$$C_O = \frac{V_O(1-D)}{\delta L_O f^2 \Delta V_O} \tag{20}$$

Table 1. Specifications of the proposed converter and its elements values

elements /specifications	art name/ value
Power switch	IRF740
Diodes	MUR860
La	10µH
L1-L2-Lo	100µH
C_C-C1-C2	10µF
Co	47µF
f_S	100kHz

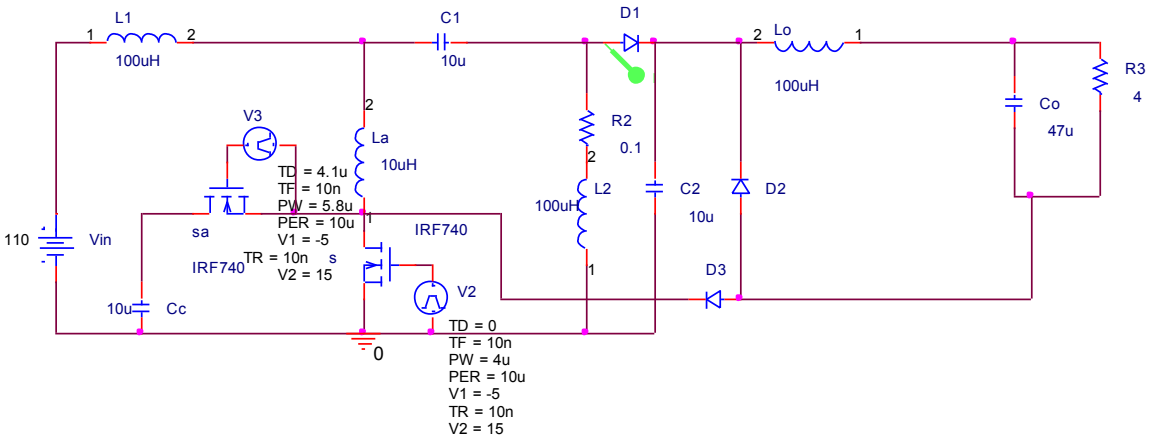

Fig. 6. Schematic view of the proposed high step-down converter simulated in PSpice software

3- 4- Calculation of auxiliary inductor L_a

To calculate the auxiliary inductor L_a, the energy equation should be used. In fact, the energy of the inductor L_a must be greater than the energy of capacitors of switches S and S_a. So:

$$\frac{1}{2}L_a I_{L1}^2 > \frac{1}{2}(C_S + C_{Sa})V_{C_C}^2 \quad (21)$$

$$L_a > \frac{(C_S + C_{Sa})V_{C_C}^2}{I_{L1}^2} \quad (22)$$

4- Simulation of the proposed high step-down converter

The proposed converter was simulated using PSpice software, targeting an output voltage of 18 volts, an input voltage of 110 volts, and a power output of 90W. Details of the designed components are outlined in Table 1, with a schematic representation of the high step-down converter shown in Fig. 6. Fig. 7 illustrates the current and voltage waveforms for the primary switch S, highlighting a negative current at the point of activation which triggers the body diode and enables zero voltage switching (ZVS) conditions. Similarly, Fig. 8 displays the waveforms for the auxiliary switch S_a, where the current is also negative upon activation, ensuring ZVS and eliminating capacitive turn-on losses. The waveform for diode D_1 in Fig. 9 indicates that its current rises and falls gradually upon activation and deactivation, respectively, achieving a zero current (ZC) condition and thus avoiding the reverse recovery issue. Moreover, Fig. 10 shows that diodes D_2 and D_3 conduct alternately under ZC conditions, preventing reverse recovery issues. Lastly, Fig. 11 reveals the output current waveform with a ripple of approximately 1.5A, significantly less than

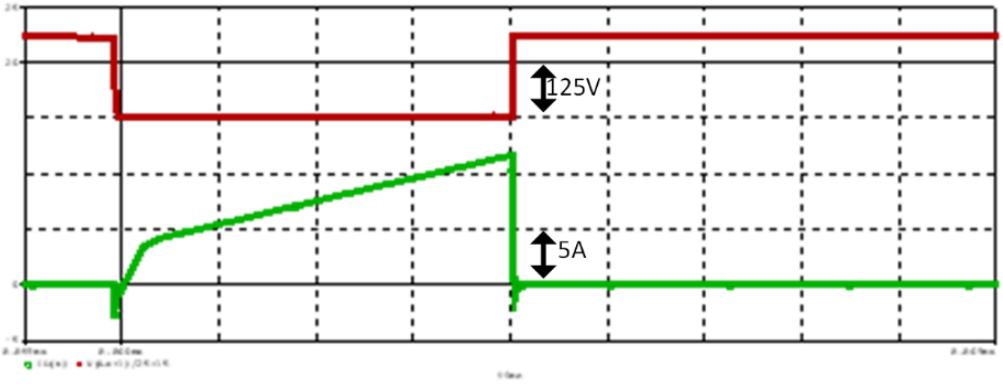

Fig. 7. Switch S current (green) and voltage (red) waveforms of the simulated converter in scale (1µs/div, 5A/div, 125V/div)

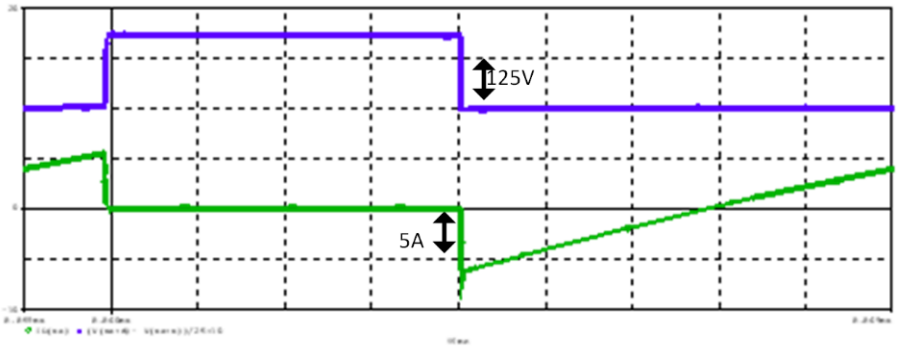

Fig. 8. Switch Sa current (green) and voltage (Blue) waveforms of the simulated converter in scale (1µs/div, 5A/div, 125V/div)

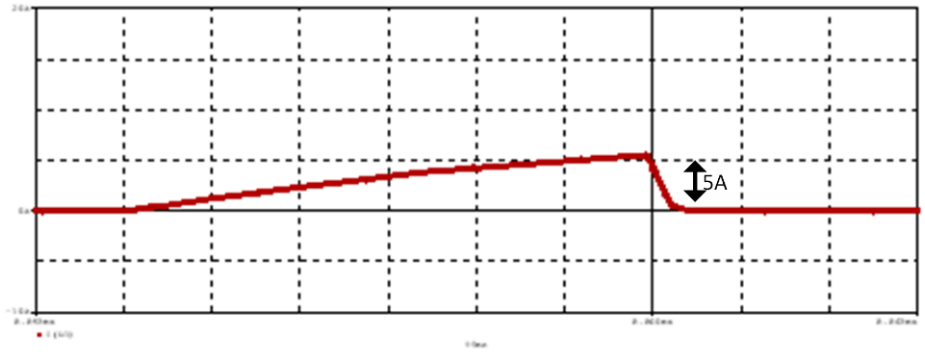

Fig. 9. Diode D_1 current waveform of the simulated converter in scale (1µs/div, 5A/div)

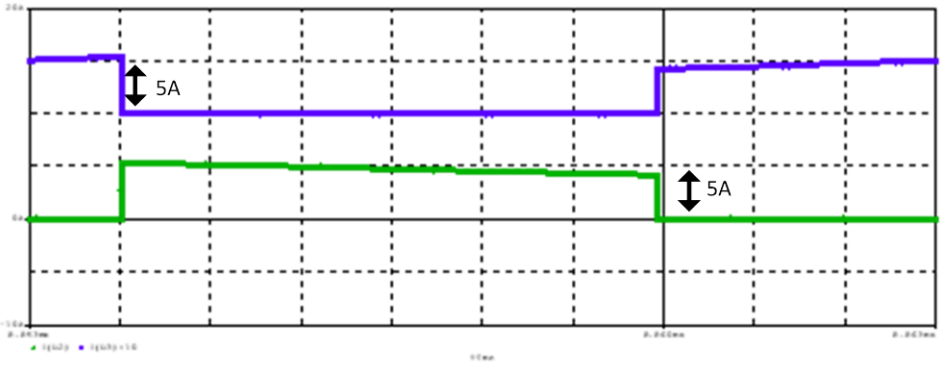

Fig. 10. Diode D_2 and D_3 current waveform of the simulated converter in scale (1µs/div, 5A/div)

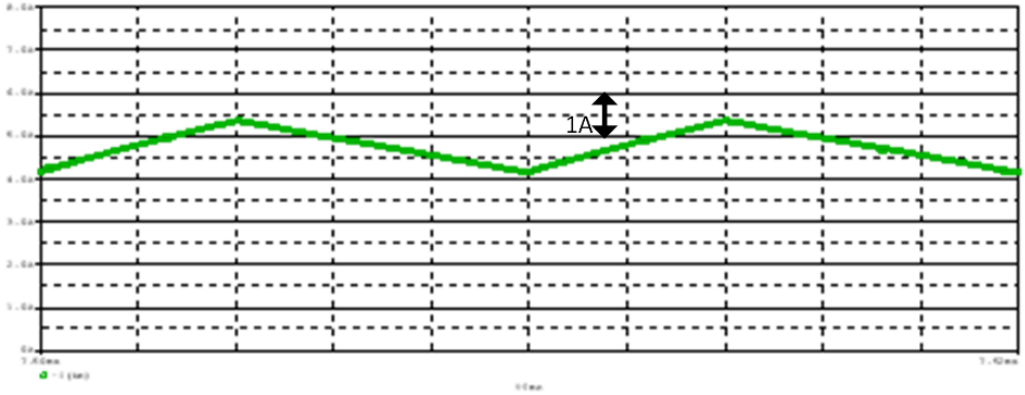

Fig. 11. The output current waveform of the simulated converter in scale (2µs/div, 0.5A/div)

what is observed with coupled inductors, though this ripple can be further minimized by increasing the output inductor's value if needed.

5- Practical results of the proposed high step-down converter

This section presents the empirical outcomes of the developed high step-down converter, which was built as per the design specifications outlined in Table 1, with its prototype in Fig. 12. The converter achieves an efficiency of 95% at a rated load of 90W. Voltage and current waveforms of the source-drain of switches S and S_a, the currents waveform of diodes D_1-D_3, and the output current waveform of the converter are shown in Fig. 13. The figures illustrate that due to the activation of the body diodes, the converter's switches achieve zero voltage switching (ZVS) prior to being turned on, and the diodes turn off under zero current (ZC) conditions. Also, Fig. 13(d) shows the output current ripple of the converter, which is 1.5 A. Hence, the practical findings validate the simulation outcomes and theoretical analyses of the circuit.

6- Comparison of the proposed converter efficiency

Fig. 14 showcases the efficiency of the proposed converter. It is observed that the converter reaches its peak efficiency of 95% at full load. However, as the load decreases and soft switching conditions are no longer maintained, the efficiency drops. At a 30W load, the efficiency is recorded at 90.5%. This indicates a 5% improvement in efficiency at full load compared to its hard-switching counterpart.

Fig. 12. Image of the proposed implemented converter

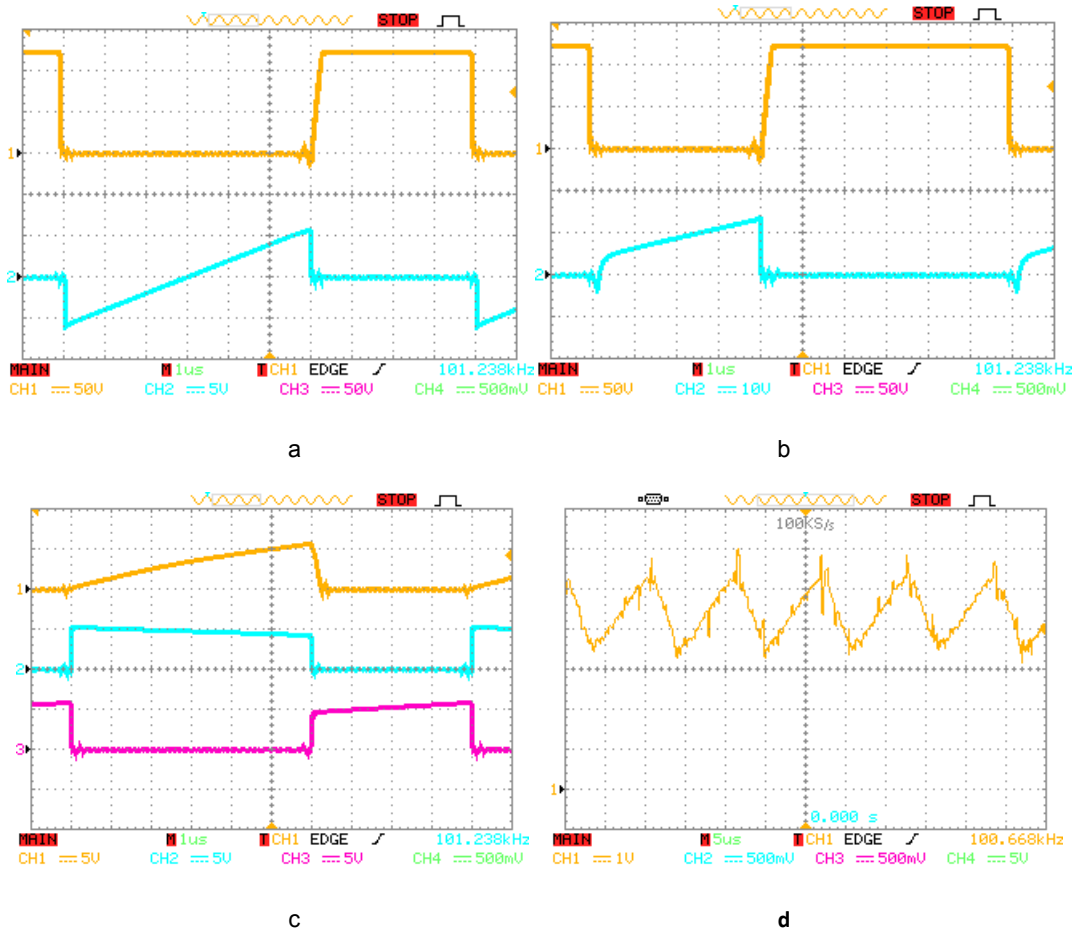

Fig. 13. Practical waveforms of the proposed converter a) Voltage and current of the auxiliary switch (50V/div, 5A/div) b) Voltage and current of main switch (50V/div, 10A/div) c) Current waveform of diodes D1-D2-D3 (5A/div) d) Output Current Waveform(1A/div)

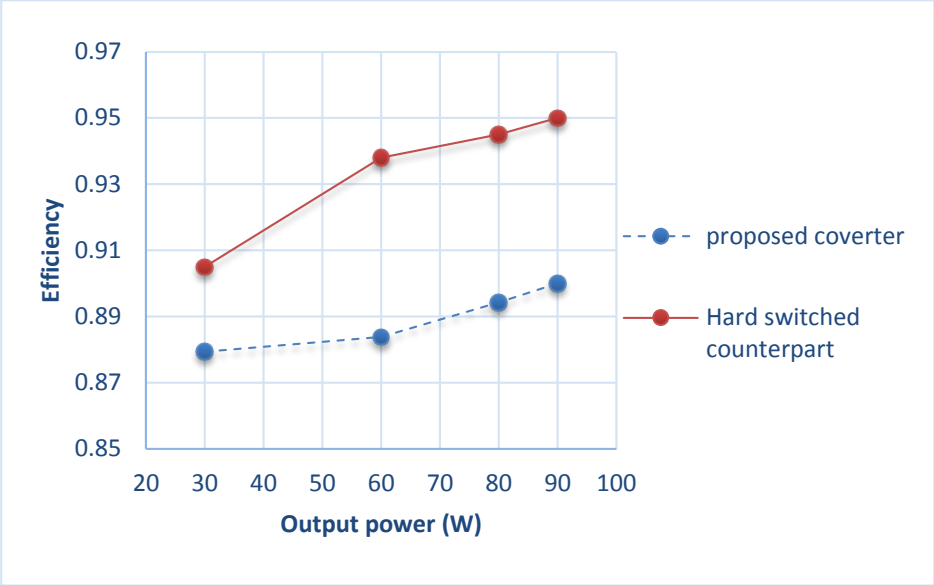

Fig. 14. Efficiency diagram of the proposed high step-down converter compared to its hard switching counterpart.

Table 2. Comparison of the proposed converter with previous converters

parameter \ reference	[19]	[8]	[14]	[11]	proposed converter
number of elements	17	15	12	9	13
switching type	Hard	ZVT	ZVT	Hard	ZVT
voltage gain	D/4	D/4(1+n)	D/2	D/2	$D^2/(n+1)$
number of switches	4	4	4	4	2
number of coupled inductors	0	1	1	1	0
output current ripple	low	high	high	low	low

7- Comparison of the proposed converter with previous similar converters

In this section, in Table 2, the proposed converter is evaluated against prior models, focusing on the count of components, voltage gain, switch quantity, and output current ripple. The proposed converter features fewer components than those cited in references [8] and [19]. Notably, Converter [19], sharing the absence of a coupled-inductor with the proposed converter, suffers from hard switching operation and elevated switching losses. Compared to the proposed converter, the Converter [11] utilizes fewer components but experiences hard switching similar to the Converter [19]. Although Converter [14] operates under Zero-Voltage (ZV) conditions with fewer components than our design, its increased number of switches complicates its operation. Conversely, despite Converter [8] presenting a more favorable voltage gain, it does so at the cost of increased switch count and current ripple compared to the proposed converter.

8- Conclusion

This paper presents a new high step-down converter that avoids using a coupled inductor, resulting in minimal current ripple at both the input and output. Its high switching frequency and the lack of a transformer contribute to its high power density. The converter features a simple design with only two switches and three diodes operating in a complementary manner, making the control circuit straightforward. Inductors at both the input and output stages help minimize current ripple throughout the converter.

Key attributes of this high step-down converter include zero voltage switching for both main and auxiliary switches, elimination of reverse recovery issues in diodes, low output, and input current ripple, and Pulse Width Modulation (PWM) control. Additionally, the design eliminates capacitive turn-on losses in switches, reduces voltage gain, extends the duty cycle, and ensures lower voltage stress on both switches and diodes. To advance the research outlined above, it is suggested to focus on several key areas for further investigation. First, developing and exploring different control strategies for the proposed converter could enhance its performance and adaptability. Additionally, adjustments to the converter's topology to allow for common ground between the input and output could improve its efficiency and integration capabilities.

9- Nomenclature

ZVT	Zero Voltage Transition
ZCS	Zero Current Switching
PWM	Pulse Width Modulation
D	Duty cycle
ICT	Information and communication technology
CI	Coupled-inductor
f	Switching Frequency

Greek symbols

μs	Microsecond
ΔV_o	Output Voltage Ripple
ΔI_o	Output Current Ripple

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