



Review Article

Advances on CMOS Folded-Cascode Operational Transconductance Amplifier: A Tutorial Review

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ABSTRACT: In this paper, a tutorial review on several structural improvements of the CMOS folded-cascode operational transconductance amplifier (OTA) is presented. After a brief discussion on the structure and operation of the conventional folded-cascode amplifier, its several architectural improvements are reviewed. These improvements include advances on class A and class AB folded-cascode amplifiers and recycling folded-cascode amplifier. Afterwards, several improved class A and class AB recycling folded-cascode operational transconductance amplifiers are discussed, and finally some two-stage operational transconductance amplifiers based on the current recycling technique are reviewed. As it can be seen, many architectural innovations have been proposed to improve both small-signal parameters, including DC gain, unity-gain bandwidth, phase margin, and large-signal operation, which is usually characterized by slew rate in the proposed OTAs compared to the basic folded-cascode amplifier. Current recycling, shunt current sources, cross-coupled transistors to realize local positive feedback paths, local common-mode feedback, flipped voltage follower cells to realize class AB operation, active current mirrors, and several other techniques have been utilized in the structural improvements of the basic folded-cascode operational transconductance amplifier. The achieved results are more promising and demonstrate substantial achievements in the design of operational transconductance amplifiers in low-voltage and more scaled nano-meter CMOS processes.

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fast settling**1- Introduction**

Operational transconductance amplifiers (OTAs) are extensively utilized in analog and mixed-signal integrated circuits. In operational amplifiers (op-amps), input impedance is large and output impedance is small in order to amplify input signal voltage, while in OTAs both input and output impedances should be large enough [1, 2]. Moreover, the op-amp is a voltage amplifier, whereas in the OTA, the input signal is voltage and the output signal is current. Therefore, the OTA is a transconductance amplifier and it is widely employed in integrated circuits where the output loads are large and usually in the form of capacitors instead of resistors. One of the main applications of OTAs is in switched-capacitor circuits. The main role of an OTA is to provide a clean virtual ground in the circuit and the accuracy of the generated virtual ground depends on the OTA DC gain.

OTAs are characterized with small-signal and large-signal performance parameters. DC gain, unity-gain frequency, phase margin, input-referred noise, power supply rejection ratio (PSRR), common-mode rejection ratio (CMRR), offset, etc, are categorized as the small-signal parameters. For large-signal operation, slew rate, total harmonic distortion (THD), and input and output signal ranges are the important

parameters. The power consumption and active silicon die area should be minimized for a target application in integrated circuits. The speed of OTAs are determined with the unity-gain frequency, slew rate, and in discrete-time applications such as the switched-capacitor circuits, the OTA output voltage should be settled within a limited time period with the required settling error.

OTAs can be realized by single-stage, two-stage, and multi-stage amplifiers. Although, DC gain is considerably enhanced by using multi-stage amplifiers, while the multi-stage OTAs stability in closed-loop configuration is a big concern. Frequency compensation techniques can be utilized to achieve a dominant pole, and hence, the stability with sufficient margin [3-10]. However, all frequency compensation techniques reduce the unity-gain bandwidth and speed of the OTA. Moreover, the analysis and design of multi-stage amplifiers are complicated, and several techniques are needed to design multi-stage OTAs for fast settling switched-capacitors [11-14].

In single-stage OTAs, there is only one high impedance node in the signal path, and hence, a dominant real pole is simply achieved without needing any frequency compensation method. Therefore, single-stage OTAs are inherently stable in the closed-loop applications. There are three main single-stage OTA structures, including telescopic-cascode, folded-

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cascode, and current mirror. The telescopic-cascode OTA has higher speed, larger DC gain, and lower input-referred noise and power consumption compared to the folded-cascode OTA. Nonetheless, the folded-cascode OTA is extensively utilized in low-voltage applications since it needs smaller power supply voltage and results in larger output voltage swing compared to the telescopic-cascode OTA. Moreover, in recent nano-meter CMOS technologies, the power supply voltage is less than one volt and the output voltage swing in telescopic-cascode OTA is negligible. Therefore, against all of the merits of the telescopic-cascode OTA, it cannot be utilized with reasonable output voltage swing in low supply voltages.

Several active current mirrors are employed in current-mirror OTAs, and DC gain can be considerably enhanced by using large ratios between the current mirror transistors. Nonetheless, this issue reduces the value of non-dominant frequency poles and zeros, resulting in degraded stability especially in high speed applications. Therefore, the gain of active current mirrors should be reduced, resulting in reduced DC gain and also unity-gain bandwidth [15]. Therefore, current-mirrors OTAs are more suitable for medium and low speed applications, and the folded-cascode OTA is preferred in high-speed applications. Nonetheless, some recent improvements on current-mirror OTAs have been reported in [16-18].

In this paper, several recent architectural improvements on the folded-cascode OTA are reviewed. The rest of the paper is organized as follows In section 2, the structure of the conventional folded-cascode OTA and its important relations are presented. Section 3 reviews several improvements on the folded-cascode OTA. The recycling folded-cascode OTA is discussed in section 4 with more details and analysis. Section 5 reviews several recent structural improvements in the recycling folded-cascode amplifier. Finally, Section 6 concludes the paper.

2- Conventional Folded-Cascode OTA

2- 1- Single-Ended Folded-Cascode OTA

Figure 1(a) shows the structure of the conventional single-ended folded-cascode OTA. The PMOS M_1 and M_2 input transistors are employed to realize the common-source input stage. The NMOS M_5 and M_6 cascode transistors are used to implement the common-gate stage. It is worth mentioning that the cascode amplifier is realized by using a common-source input stage, following by a common-gate stage known as the cascode stage. The type of common-source and cascode transistors cannot be the same. Normally, PMOS input transistors are preferred over NMOS for achieving lower input common-mode voltage, lower input-referred flicker noise, and higher non-dominant pole, and hence, larger unity-gain bandwidth.

The DC gain and associated frequency poles and zeros to the signal nodes of the single-ended folded-cascode amplifier (FCA) are given by:

$$\begin{aligned}
 A_{dc} &\approx g_{m1} R_{out} \approx \\
 &g_{m1} \left[g_{m6} r_{ds6} (r_{ds2} \parallel r_{ds4}) \parallel g_{m8} r_{ds8} r_{ds10} \right] \\
 \omega_L &= \frac{1}{R_{out} C_L}, \quad \omega_C \approx \frac{g_{m9}}{C_B}, \\
 \omega_A &\approx \frac{g_{m6}}{C_A}, \quad \omega_B \approx \frac{g_{m5}}{C_B}
 \end{aligned} \tag{1}$$

where C_L, C_A, C_B, C_C are the output load capacitance, total parasitic capacitors at the nodes $A, B,$ and $C,$ respectively. g_m and r_{ds} denote the small-signal transconductance and drain-source resistance of the corresponding transistors, respectively. Since there are two different signal paths from input to the output, the OTA transfer function is given by:

$$A_d(s) = \frac{A_1}{(1+s/\omega_L)(1+s/\omega_A)} + \frac{A_2}{(1+s/\omega_L)(1+s/\omega_B)(1+s/\omega_C)} \tag{2}$$

Since $\omega_A \approx \omega_B$ and DC gain of both paths is the same, the transfer function is simplified as follows:

$$A_d(s) = A_{dc} \frac{(1+s/2\omega_C)}{(1+s/\omega_L)(1+s/\omega_A)(1+s/\omega_B)} \tag{3}$$

Therefore, the frequency poles and zeros and unity-gain frequency are obtained as:

$$\begin{aligned}
 \omega_{p1} = \omega_L &= \frac{1}{R_{out} C_L}, \quad \omega_{p2} = \omega_C \approx \frac{g_{m9}}{C_B}, \\
 \omega_{p3} = \omega_A &\approx \frac{g_{m6}}{C_A}, \quad \omega_{z1} \approx -\frac{2g_{m9}}{C_A} \\
 \omega_t \approx A_{dc} \omega_{p1} &\Rightarrow \omega_t = \frac{g_{m1}}{C_L}
 \end{aligned} \tag{4}$$

As it is clear, the single-ended FCA has one dominant and two non-dominant poles and one Left half plan (LHP) zero. By using equal bias current in input and cascode transistors as shown in Fig. 1(a), both positive and negative slew rates are simply given by:

$$SR = \frac{2I_b}{C_L} \tag{5}$$

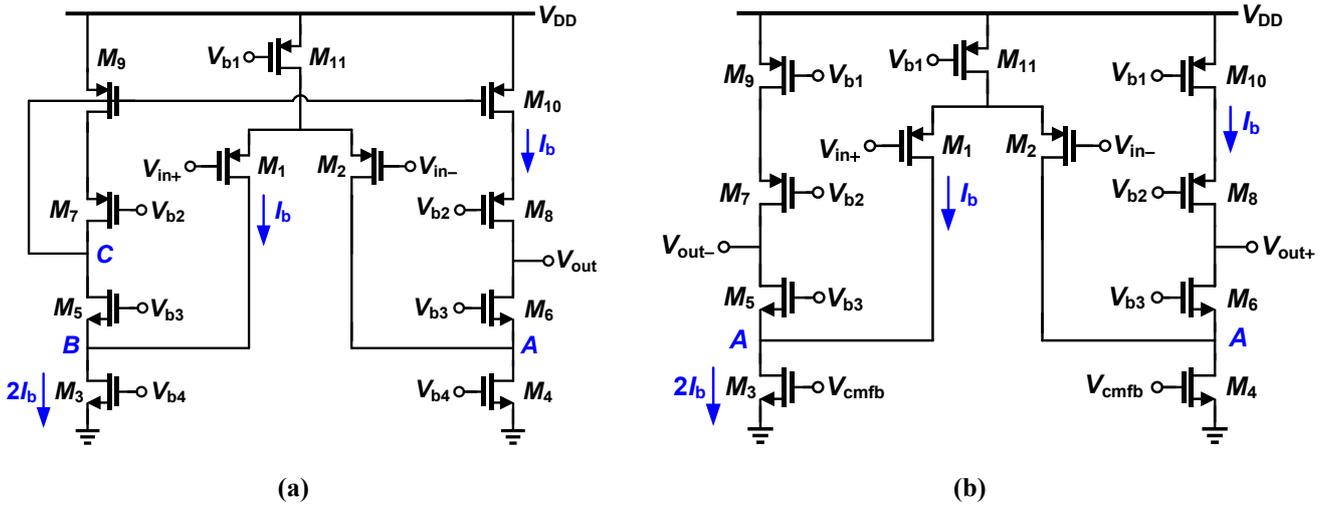


Fig. 1. (a) Conventional single-ended and (b) fully-differential folded-cascode OTAs.

By considering both thermal and flicker noise of the MOS transistors, the power spectral density (PSD) of the input-referred noise of the single-ended FCA is simply calculated as:

$$V_{n,in}^2(f) = \frac{8kT\gamma}{g_{m1}} \left[1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}} \right] + \left[\frac{2K_{fp}}{W_1L_1C_{ox}f} + \frac{2K_{fn}}{W_3L_3C_{ox}f} \left(\frac{g_{m3}}{g_{m1}} \right)^2 + \frac{2K_{fp}}{W_9L_9C_{ox}f} \left(\frac{g_{m9}}{g_{m1}} \right)^2 \right] \quad (6)$$

where k is the Boltzmann's constant, γ is the thermal noise excess factor, and W and L are the channel width and length of the transistors, respectively. K_{ip} and K_{in} are the flicker noise coefficient in PMOS and NMOS transistors, respectively. It is worth mentioning that the noise effect of cascode transistors is negligible owing to the source degeneration in these transistors.

2- 2- Fully-Differential Folded-Cascode OTA

Figure 1(b) shows the structure of the fully-differential folded-cascode OTA. Here, the input stage is realized by PMOS input pair, and NMOS M_5 and M_6 transistors are employed as the cascode transistors. DC gain, unity-gain frequency, slew rate, and input-referred noise are the same as the single-ended FCA while it has only two frequency poles without any zero, as follows:

$$\omega_{p1} = \frac{1}{R_{out}C_L}, \quad \omega_{p2} \approx \frac{g_{m5}}{C_A} \quad (7)$$

The common-mode response of the fully-differential OTAs is superior compared to the single-ended counterparts in terms of CMRR and PSRR. However, instead of the single-ended FCA, the fully-differential one needs a common-mode feedback (CMFB) circuit to define the common-mode voltage of the output nodes in the closed-loop configuration, since the feedback network cannot set the input and output common-mode voltages of the OTA. The control voltage of the CMFB circuit can be applied to the gate of M_3 and M_4 , M_9 and M_{10} , and M_{11} transistors. As shown in Fig. 1(b), it is usually applied to the gate of M_3 and M_4 current source transistors, since in this case larger gain is achieved in CMFB loop with less frequency poles and zeros, and hence, better stability in CMFB loop in high speed applications.

According to Fig. 1, the drain current of M_3 and M_4 transistors is twice the drain current of other transistors, especially input and cascode transistors, while these transistors are only acting as the current sources without any role in the amplification path. This is the main drawback of both single-ended and fully-differential folded-cascode OTAs, and in most of the improved folded-cascode OTAs, M_3 and M_4 current source transistors are also utilized in the signal amplification path to increase both small-signal and large-signal parameters. In the next sections, several structural advances on the operation of folded-cascode OTA are reviewed.

3- Advances on Folded-Cascode OTA

3- 1- Improved Folded-Cascode OTAs

Figure 2 shows an enhanced fully-differential FCA, where additional M_{5a} - M_{10a} transistors are utilized to improve the DC gain and CMRR without any sacrificing in slew rate [19]. Here, M_9 - M_{10} current sources in conventional FCA are also employed in the signal amplification path. Owing

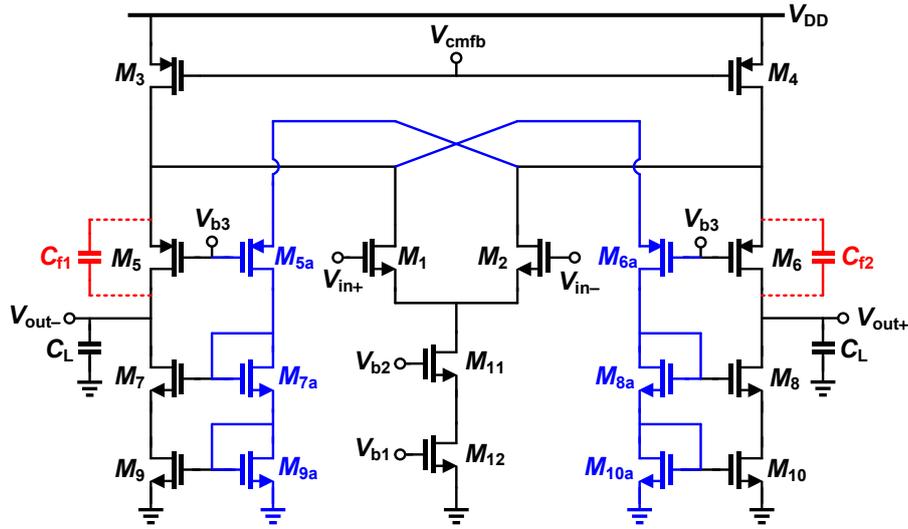


Fig. 2. Enhanced fully-differential folded-cascode OTA [19].

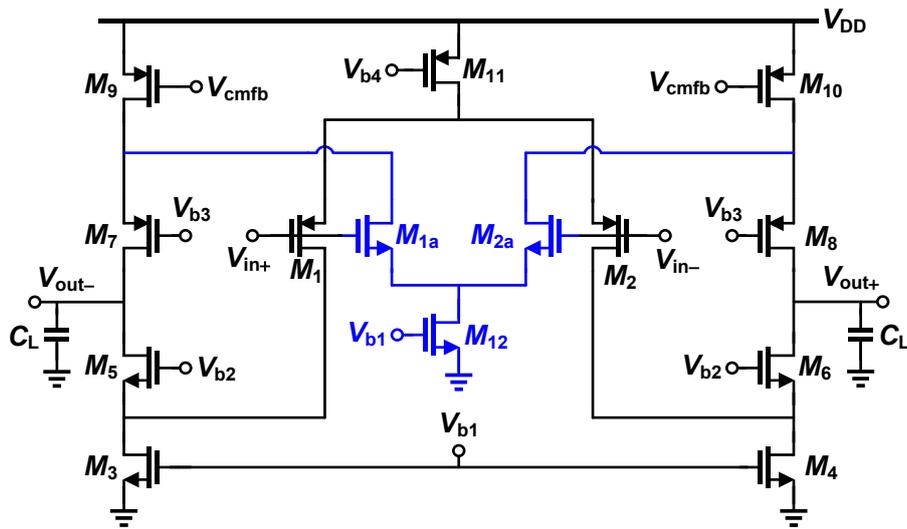


Fig. 3. Complementary fully-differential folded-cascode OTA [20, 21].

to the added transistors at the cascode nodes (drain of M_1 and M_2 transistors), the non-dominant pole is reduced and this can degrade the stability. This issue has been alleviated using C_{f1} and C_{f2} feedforward capacitors across the cascode transistors, as shown in Fig. 2. Actually, this OTA has been comprised of two separated folded-cascode amplifiers where M_1 - M_2 are the input transistors in both amplifiers, and M_5 - M_6 and M_{5a} - M_{6a} are the main and added cascode transistors, respectively. The drain current of M_3 - M_4 current sources are utilized to bias the input and all cascode transistors. The differential DC gain of two amplification paths is added in phase while their common-mode gain is subtracted, resulting in larger differential gain and reduced common-mode gain. Its differential transfer function has one dominant pole at the

output node and two non-dominant poles and a LHP zero, owing to having two different paths from the input to the output with different delays.

In [20, 21], complementarily differential pairs (one NMOS and one PMOS) are utilized as the input transistors in FCA, as shown in Fig. 3. Here, the drain current of both NMOS and PMOS current sources are utilized to bias both input and cascode transistors, and this improves DC gain and bandwidth of OTA compared to the conventional FCA with the same power consumption. The drain current of idle current sources is efficiently employed to provide an additional gain path. Moreover, this is a two-path OTA comprising of two conventional folded-cascode OTAs with one PMOS and one NMOS input transistors. The differential gain of both FCAs

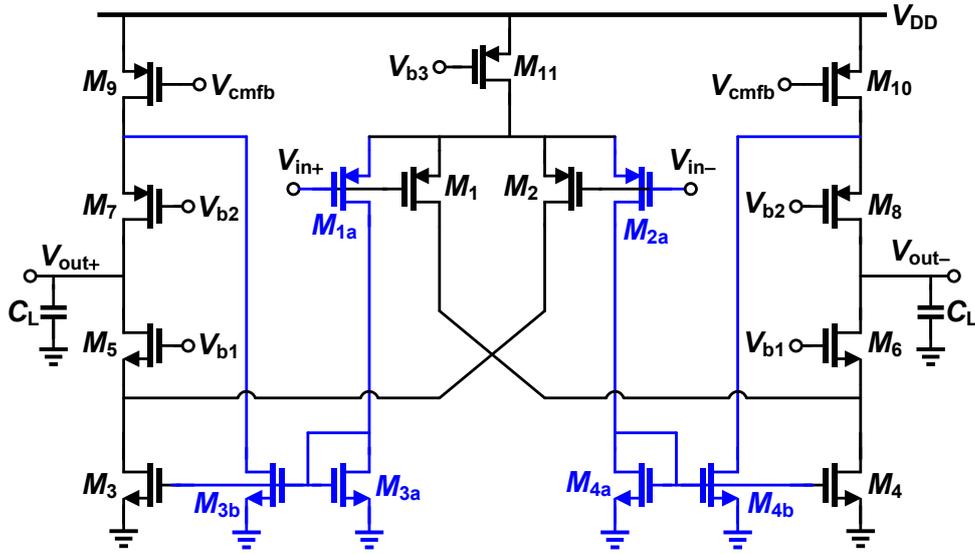


Fig. 4. Three-path OTA [22].

is added in phase resulting in larger DC gain.

In [22], as shown in Fig. 4, a three-path OTA has been proposed where one folded-cascode OTA, one current-mirror OTA, and one current-mirror folded-cascode OTA are employed. The conventional FCA is realized by M_1 - M_{11} transistors. An additional PMOS input pair (M_{1a} - M_{2a}) is utilized to build two other paths. The current-mirror OTA is realized by M_{1a} - M_{2a} , M_{3a} - M_{4a} , and M_3 - M_4 transistors. The third signal amplification path, which is a combination of current-mirror with folded-cascode, is implemented by M_{1a} - M_{2a} , M_{3a} - M_{4a} , M_{3b} - M_{4b} , and M_7 - M_8 transistors. this way, the drain current of M_3 and M_4 current sources are also completely utilized in the signal amplification path, and the drain current of M_9 and M_{10} current sources are employed to bias both M_7 - M_8 PMOS cascode transistors and M_{3b} - M_{4b} active current mirrors. Compared to the conventional FCA, both small-signal and large-signal parameters are considerably improved with the same power consumption.

3- 2- Class AB Folded-Cascode OTAs

In class A OTAs, the drain current of all transistors is limited when a large differential input signal is applied to the OTA input. However, in class AB OTAs, the amplifier is biased with a quiescent current, and the drain current of input transistors are considerably increased when a large input signal is applied. This issue is important in fast settling applications, such as switched-capacitor circuits, since the OTA is intended to settle in a definite time with a targeted settling error. Thus, the slew rate of class AB OTAs is larger than class A ones. The class AB operation can be used in both input and output stages of a folded-cascode OTA.

A folded-cascode amplifier with class AB operation in both input and output stages has been presented in [23, 24] which is illustrated in Fig. 5. The class AB operation in input stage is realized by flipped voltage follower (FVF) cells [25]. The gate of M_{C5} and M_{C6} transistors are connected to the gate of M_{10} and M_9 current source transistors, respectively, to also bring them in the signal amplification. By this simple technique, DC gain, unity-gain frequency, and both positive and negative slew rates are considerably improved resulting in reduced settling time in switched-capacitor circuits. According to the detailed simulation results in [23], compared to the conventional FCA, using the proposed class AB operation only in input stage improves DC gain about 6.5 dB, unity-gain frequency about 75%, 35% reduction in settling time, and without any slew rate improvement with the same power consumption and reduced phase margin. However, by using the class AB operation in both input and output stages, both small-signal and large-signal parameters are significantly improved.

A current-mirror class AB OTA has been presented in [26]. Although DC gain, unity-gain frequency, and slew rate have been considerably increased compared to the conventional current-mirror OTA, it is a single-ended amplifier and the utilized techniques can be less efficient in the fully-differential current-mirror OTA.

Figure 6 shows the proposed class AB folded-cascode OTA in [27]. In this OTA, the input signal is capacitively coupled to the gate of output current sources. Hence, class AB operation is realized in output current source transistors without needing any static power dissipation. Both small-signal and large-signal changes of the input signal are directly

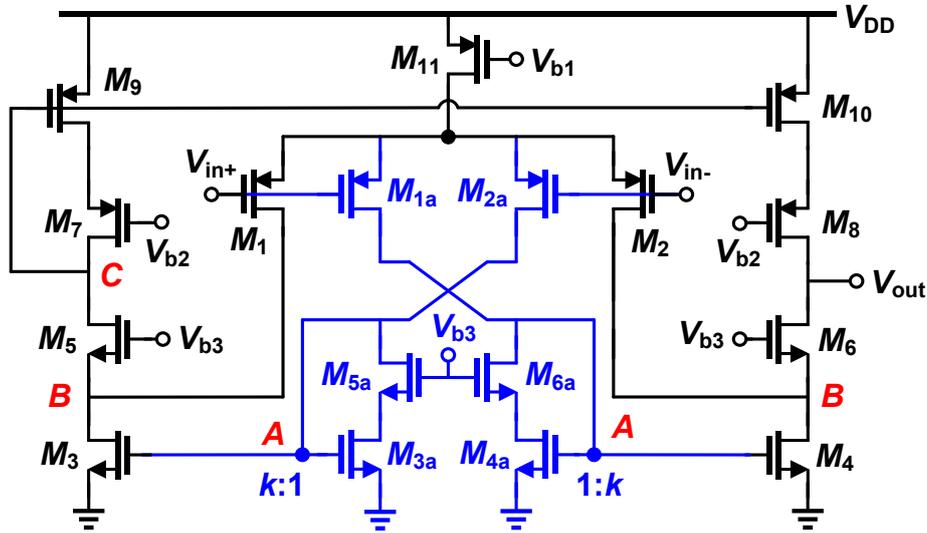


Fig. 7. Single-ended recycling folded-cascode OTA [32-34].

coupled to the gate of M_3 - M_4 and M_9 - M_{10} transistors, resulting in significantly improved DC gain, unity-gain bandwidth, and slew rate. To bias the M_3 - M_4 and M_9 - M_{10} transistors, their gate terminal is connected to the proper bias voltages through diode-connected M_{r1} - M_{r4} PMOS transistors. M_{r1} - M_{r4} transistors are in cut-off region and provide a very large resistance with small aspect ratio. Furthermore, the bulk of these transistors is connected to their sources in order to avoid the bulk-source junction leakage, and hence, reduction of their resistance. The DC gain is reduced at low frequencies owing to the usage of C_{b1} - C_{b4} capacitors at signal path. Therefore, this OTA has a band-pass characteristic. Nonetheless, the lower cut-off frequency can be less than a few hertz by using large bias resistors. Based on the detailed simulation results presented in [27], both small-signal and large-signal parameters of this class AB OTA have been significantly improved compared to the conventional FCA and the resulting settling time has been reduced about 3.7 times.

A class AB single-ended folded-cascode OTA has been proposed in [28] to drive large capacitive loads. In this OTA, class AB operation is realized by using FVF cells at input transistors. Adaptive biasing is utilized in both input and current folding transistors to provide class AB operation with dynamic current boosting and enhanced gain-bandwidth. In [29], a fully-differential FCA with dynamic current boosting paths and FVF cells has been presented to realize a class AB OTA with improved small-signal transconductance and settling performance. Two nested positive and negative

feedback loops have been employed at the active loads of an adaptively biased input stage in [30] to realize a super class AB OTA with both improved small-signal and large-signal performances.

In most class AB OTAs, the tail current source is replaced with FVF cells. Thus, the small-signal resistance at the common source node of input transistors is significantly reduced, and hence, the common-mode response is considerably degraded. In [31], an additional circuit is utilized to cancel the common-mode components at the output nodes, and thus, to improve the common-mode response. This way, the common-mode gain has been reduced about 40 dB without affecting the differential-mode parameters.

4- Recycling Folded-Cascode OTA

4- 1- Single-Ended Recycling Folded-Cascode OTA

Figure 7 shows the structure of single-ended recycling folded-cascode OTA [32-34]. In this OTA, the input transistors are split as M_1 , M_2 , M_{1a} and M_{2a} in order to exploit the idle M_3 and M_4 current source transistors in the conventional FCA into the signal path. Actually, the recycling FCA (RFCA) is comprised of one conventional FCA and one current-mirror OTA. M_1 - M_{11} transistors are used to build the conventional FCA, and the current-mirror OTA is implemented by M_{1a} , M_{2a} , M_{3-11} transistors.

The small-signal parameters of the single-ended RFCA are given by:

$$\begin{aligned}
A_{dc} &\approx (g_{m2} + kg_{m1a})R_{out} \\
R_{out} &\approx g_{m6}r_{ds6}(r_{ds2} \parallel r_{ds4}) \parallel g_{m8}r_{ds8}r_{ds10} \\
\omega_{out} &= \frac{1}{R_{out}C_L}, \quad \omega_A \approx \frac{g_{m3a}}{C_A}, \\
\omega_B &\approx \frac{g_{m5}}{C_B}, \quad \omega_C \approx \frac{g_{m9}}{C_C} \\
\omega_t &\approx A_{dc}\omega_{out} \approx \frac{(g_{m2} + kg_{m1a})}{C_L}
\end{aligned} \tag{8}$$

Additionally, its small-signal transfer function is obtained as:

$$\begin{aligned}
A_v(s) &= \frac{A_1 = 0.5g_{m1}R_{out}}{(1+s/\omega_B)(1+s/\omega_C)(1+s/\omega_{out})} + \\
&\frac{A_2 = 0.5kg_{m1a}R_{out}}{(1+s/\omega_A)(1+s/\omega_{out})} + \\
&\frac{A_3 = 0.5kg_{m2a}R_{out}}{(1+s/\omega_A)(1+s/\omega_C)(1+s/\omega_{out})} + \\
&\frac{A_4 = 0.5g_{m2}R_{out}}{(1+s/\omega_B)(1+s/\omega_{out})} \Rightarrow \\
A_v(s) &= \frac{N(s)}{(1+s/\omega_A)(1+s/\omega_B)(1+s/\omega_C)(1+s/\omega_{out})}
\end{aligned} \tag{9}$$

where $N(s)$ is as follows:

$$\begin{aligned}
N(s) &= (A_1 + A_2 + A_3 + A_4) + \\
&s \left[\frac{A_1}{\omega_A} + \frac{A_2}{\omega_B} + \frac{A_2}{\omega_C} + \right] + \\
&s^2 \left[\frac{A_2}{\omega_B\omega_C} + \frac{A_4}{\omega_A\omega_C} \right]
\end{aligned}$$

Therefore, it has four poles and two zeros. The single-ended RFCA has symmetric slewing behavior, and both positive and negative slew rates are given by:

$$SR = \frac{kI_{D11}}{C_L} \tag{10}$$

Compared to the conventional FCA, by using the same aspect ratio in input transistors and equal power consumption, the value of k should be 3. Therefore, their small-signal and large-signal parameters are related as where indices FC and

RFCA belong to the FCA and RFCA, respectively.

$$\begin{aligned}
\omega_{t,RFCA} &= 2\omega_{t,FC}, \quad A_{dc,RFCA} > 2A_{dc,FC}, \\
SR_{RFCA} &= 3SR_{FC}
\end{aligned} \tag{11}$$

As it is clear, the unity-gain frequency and slew rate improvements of RFCA are 2 and 3, respectively. DC gain enhances more than twice owing to the reduction of bias current in output transistors, which increases the output resistance. Nonetheless, the phase margin of RFCA is degraded due to the added poles. However, this is not important since the FCA phase margin is very large (above 80 degree) and its reduction can be also useful in fast settling applications, where the phase margin should be between 60 to 70 degrees.

4- 2- Fully-Differential Recycling Folded-Cascode OTA

Figure 8 shows the structure of fully-differential RFCA. Here, the same technique is used to bring M_3 and M_4 current source transistors into the signal path. The small-signal parameters are given by:

$$\begin{aligned}
A_{dc} &\approx (g_{m2} + kg_{m1a})R_{out} \\
R_{out} &\approx g_{m6}r_{ds6}(r_{ds2} \parallel r_{ds4}) \parallel g_{m8}r_{ds8}r_{ds10} \\
\omega_{out} &= \frac{1}{R_{out}C_L}, \quad \omega_A \approx \frac{g_{m3a}}{C_A}, \quad \omega_B \approx \frac{g_{m5}}{C_B} \\
\omega_t &\approx A_{dc}\omega_{out} \approx \frac{(g_{m2} + kg_{m1a})}{C_L}
\end{aligned} \tag{12}$$

The small-signal transfer function is also obtained as:

$$\begin{aligned}
A_v(s) &= \frac{A_1 = g_{m1}R_{out}}{(1+s/\omega_B)(1+s/\omega_{out})} + \\
&\frac{A_2 = kg_{m2a}R_{out}}{(1+s/\omega_A)(1+s/\omega_{out})} \Rightarrow \\
A_v(s) &= \frac{(A_1 + A_2) + s \left[\frac{A_1}{\omega_A} + \frac{A_2}{\omega_B} \right]}{(1+s/\omega_A)(1+s/\omega_B)(1+s/\omega_{out})}
\end{aligned} \tag{13}$$

Therefore, it has one dominant pole at output node, two non-dominant poles, and one LHP zero. Compared to the single-ended RFCA, it has one less pole and one less zero with the same DC gain and unity-gain frequency. Additionally, the phase margin of the fully-differential RFCA is higher than its single-ended counterpart. The positive and negative slew rates of the fully-differential RFCA are obtained as:

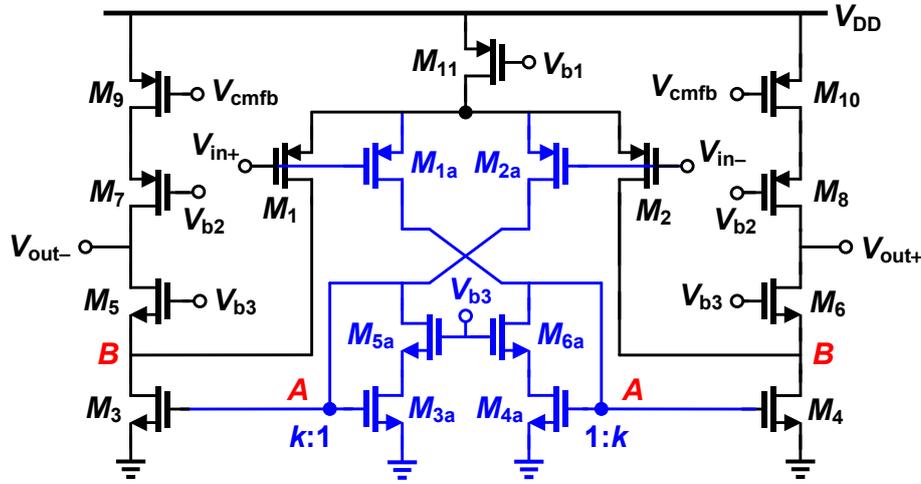


Fig. 8. Fully-differential recycling folded-cascode OTA.

$$\begin{aligned}
 SR^+ &= \frac{I_{D8}}{C_L} = \frac{(k-1)I_{D11}}{4C_L} = \frac{I_{D11}}{2C_L} \\
 SR^- &= \frac{I_{D3} - I_{D7}}{C_L} = \frac{(3k+1)I_{D11}}{4C_L} = \frac{2.5I_{D11}}{C_L}
 \end{aligned}
 \tag{14}$$

As it is clear, the slewing behavior of fully-differential RFCA is not symmetric, since in this OTA the drain current of M_7 - M_{10} cascode current source transistors is constant and it is not changed during slewing. This issue imbalances the output nodes of OTA during the slewing phase, and hence, results in increased nonlinearity.

The control voltage of CMFB circuit is usually applied to the gate of M_9 and M_{10} transistors, as shown in Fig. 8. If it is applied to the gate of M_{11} transistor, there are two CMFB paths with different gain signs. Considering $k = 3$ and equal size in input transistors, the gain from the gate of M_{11} to the output nodes will be positive, and hence, an extra inverting amplifier is needed to stabilize the CMFB loop.

In [35], the input transistors in the conventional telescopic-cascode OTA has been split to build a two-path OTA, which is comprised of telescopic-cascode and folded-cascode OTAs. A fully-differential recycling telescopic-cascode OTA has been introduced in [36]. In this OTA, the input transistors are split to realize an additional current-mirror OTA along with the telescopic-cascode one. Moreover, the current recycling and cross-coupled transistors with local positive feedback technique have been employed to considerably improve both small and large signal parameters.

5- Advances on Recycling Folded-Cascode OTAs

5- 1- Improved Recycling Folded-Cascode OTAs

Figure 9 shows the structure of the improved single-ended recycling folded-cascode OTA, which has been presented in [37]. In this OTA, M_{3b} - M_{6b} transistors are added in RFCA to separate AC and DC paths from each other in the active current mirrors, similar to the method that has been already used in [15]. This way, DC current of M_{3a} - M_{6a} transistors is reduced while their small-signal current is the same as the input transistors. Hence, DC gain and unity-gain frequency is enhanced in comparison with the RFCA as well as its slew rate. Nonetheless, this is a single-ended OTA and its fully-differential structure suffers from the asymmetric behavior in slew rate like the RFCA.

In [38], in the fully-differential RFCA, the output resistance increases by employing cross-coupled transistors at the PMOS output current sources, and hence, DC gain is enhanced. In [39], the input transistors are split to three differential pairs to realize a double recycling FCA, and shunt current sources in Fig. 9 are replaced with active current mirrors. Two input differential pairs are utilized like RFCA and the third input pair is used to drive the active current mirrors. This way, the shunt bias currents are reused twice to further increase the performance of OTA without any power and area overheads. The double recycling method has also been more developed in [40, 41, 42]. In [40], the double recycling technique, shunt active current sources, and additional drivers are utilized to achieve a single-stage multi-path fully-differential OTA with improved performance.

In [43], the current sources in [37] are replaced with cross-coupled transistors, making a local positive feedback path. The phase margin of conventional RFCA has been

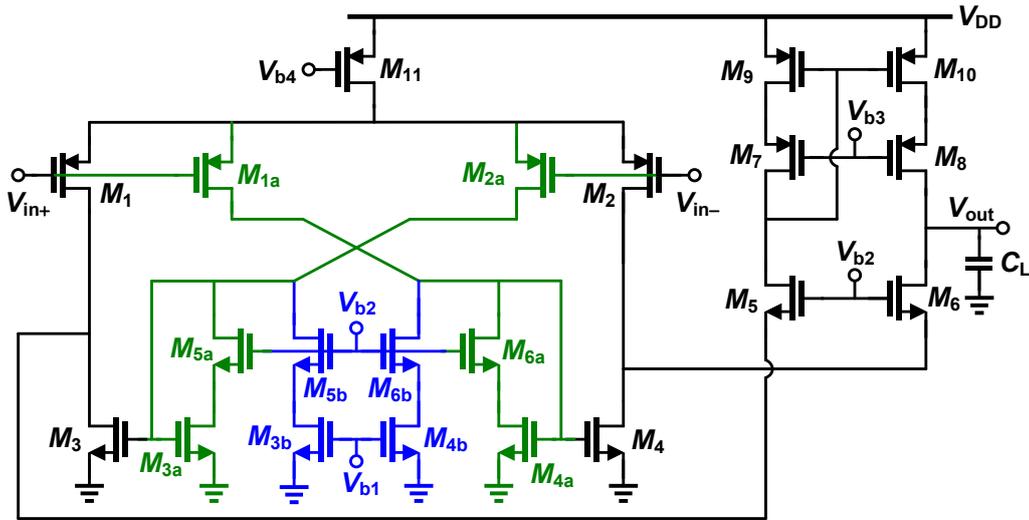


Fig. 9. Improved recycling folded-cascode OTA [37].

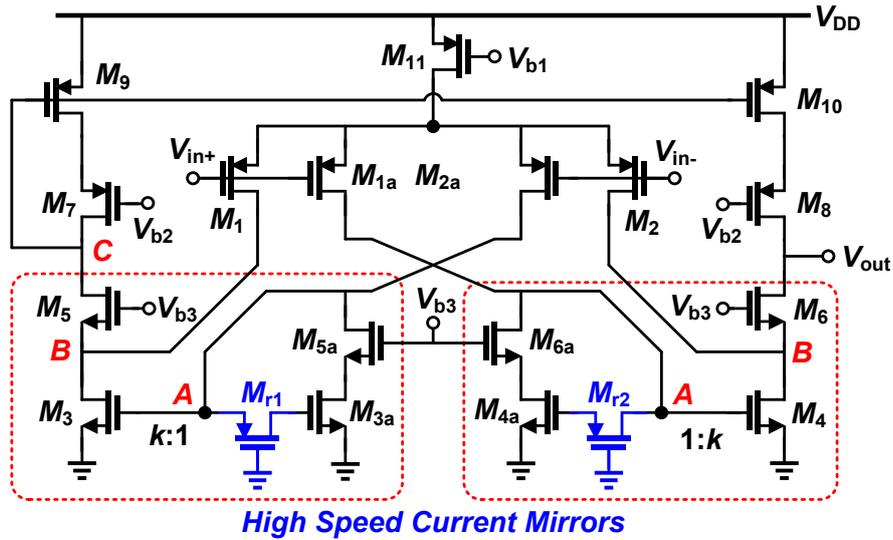


Fig. 10. Recycling folded-cascode OTA with improved phase margin [44].

improved in [44] by using high-speed current mirrors, as shown in Fig. 10. In this OTA, M_{r1} and M_{r2} transistors, which are biased in deep triode region, are employed to implement two compensation resistors that are placed in series between the gate of current mirror pairs. This way, the first non-dominant pole is cancelled with the added zero resulting in an enhanced phase margin.

A DC gain enhancement technique has been introduced in [45], where the cascode nodes in PMOS output current sources are utilized to drive the gate of main cascode transistors in a

single-ended RFCA. This way, a positive feedback path is created at the output nodes, making the output resistance to be increased. Cross-coupled transistors are added in split input pairs of a RFCA to realize the local positive feedback loops in [46]. Hence, the transconductance and DC gain of the resulting OTA are significantly improved. A constant g_m rail-to-rail OTA based on the recycling folded-cascode amplifier has been proposed in [47]. In [48], a high voltage recycling folded-cascode OTA has been suggested by employing double cascode current sources at the output nodes to tolerate large

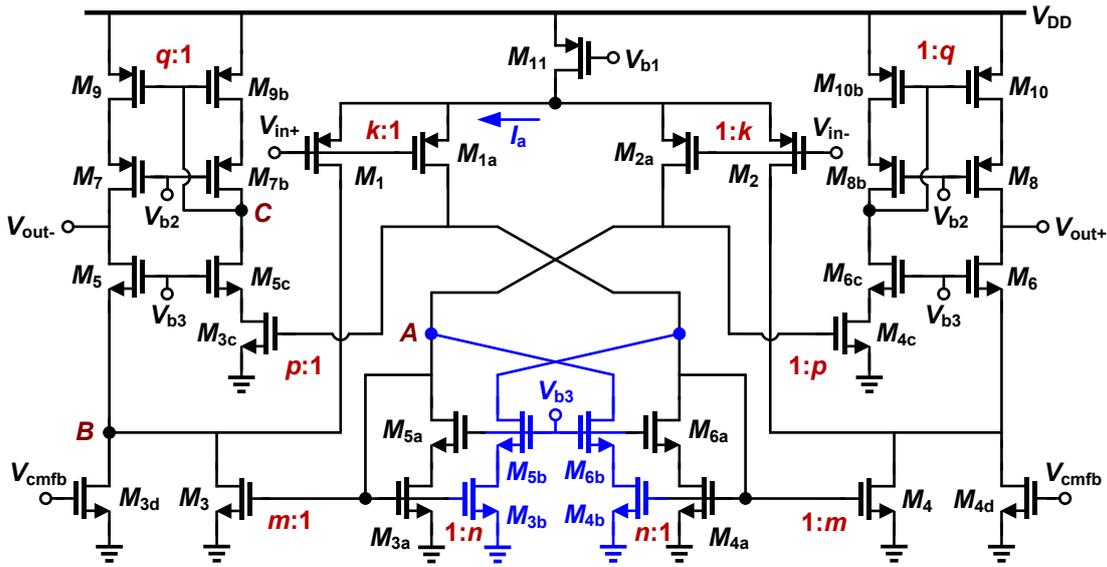


Fig. 11. Single-stage multi-path OTA [49].

power supply voltage in standard CMOS technologies.

According to detailed analysis presented in [49], the cross-coupled positive feedback transistors improve both small-signal and large-signal parameters as well. The proposed multi-path OTA in [49] is illustrated in Fig. 11. It has been comprised of one folded-cascode OTA, two current-mirror OTAs with M_{3b} - M_{4b} positive feedback cross-coupled transistors. The M_1 - M_{11} transistors realize the folded-cascode OTA. The input transistors are split as M_1 , M_2 , M_{1a} , and M_{2a} in order to employ M_3 and M_4 NMOS current source transistors in the conventional folded-cascode OTA into the signal path. The wide-swing cascode current mirrors are utilized in all active current mirrors to improve the current matching, and enhance the output resistance and DC gain. The control voltage of the CMFB circuit is applied to the gate of the added M_{3d} and M_{4d} transistors. It is worth mentioning that it cannot be directly applied to the gate of M_{11} transistor, since we have three different paths with different gain signs, and an extra power hungry intervening amplifier is needed in the CMFB loop. According to the detailed analysis and simulation results in [49], the proposed OTA improves DC gain, unity-gain frequency, and slew rate about 740%, 450%, 320%, respectively, compared to the conventional folded-cascode OTA with the same power consumption and aspect ratio in input transistors.

In [50], a fast signal path has been added in the full-differential RFCA to realize a LHP zero, and hence, to improve the phase margin and stability. The similar technique in [45] has been used in [51] to improve DC gain. Moreover, the PMOS current source transistors have been used in the signal path and high-speed current mirrors have been employed to improve the phase margin in this OTA. In [52], based on the improved RFCA shown in Fig. 9, the gain boosting technique

is utilized in both NMOS and PMOS output current sources. Furthermore, similar to [44], the phase margin is improved by using two series resistors (realized by MOS transistors in the linear region) between the gates of $M_{3,4}$ and $M_{3a,4a}$ transistors in Fig. 9.

Figure 12 shows the proposed OTA in [53] which is based on the local common-mode feedback and recycling folded-cascode amplifier. In DC and common-mode conditions, the voltage at nodes X and Y is the same and there is not any current flow in resistors R_1 and R_2 . Therefore, the gate-source voltage of transistors $M_{3,4}$ and $M_{3a,4a}$ is equal and their drain current depends on their aspect ratios. However, in small-signal operation, the voltage at node Z is zero, and hence, the transistors M_3 and M_4 operate as the common-source structure. Therefore, DC gain, unity-gain frequency, and slew rate of this OTA is considerably improved compared to the conventional RFCA. Nonetheless, this improvement depends on the value of R_1 and R_2 resistors, and the first non-dominant pole is reduced in proportion with the resistors resulting in more degraded phase margin.

The slew rate of fully-differential RFCA has been boosted in [54] using some extra paths. The added transistors are in the cut-off region in small-signal operation, and are turned-on during the slewing phase. A fully-differential RFCA has been presented in [55] with improved slew rate, DC gain and unity-gain bandwidth. The complementary PMOS and NMOS input differential pairs have been utilized in a fully-differential RFCA in [56], resulting in enhanced gain bandwidth. Using a constant DC voltage source between the source of the input pairs, an asymmetrical current split in input transistors of a single-ended RFCA has been utilized in [57] to improve the small-signal transconductance and DC gain. In [58], the local positive feedback technique has been employed in the

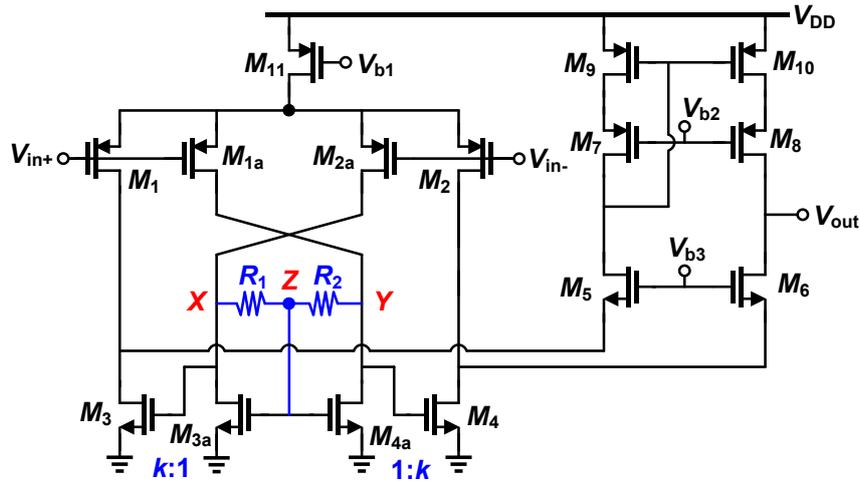


Fig. 12. Recycling folded-cascode OTA with local CMFB [53].

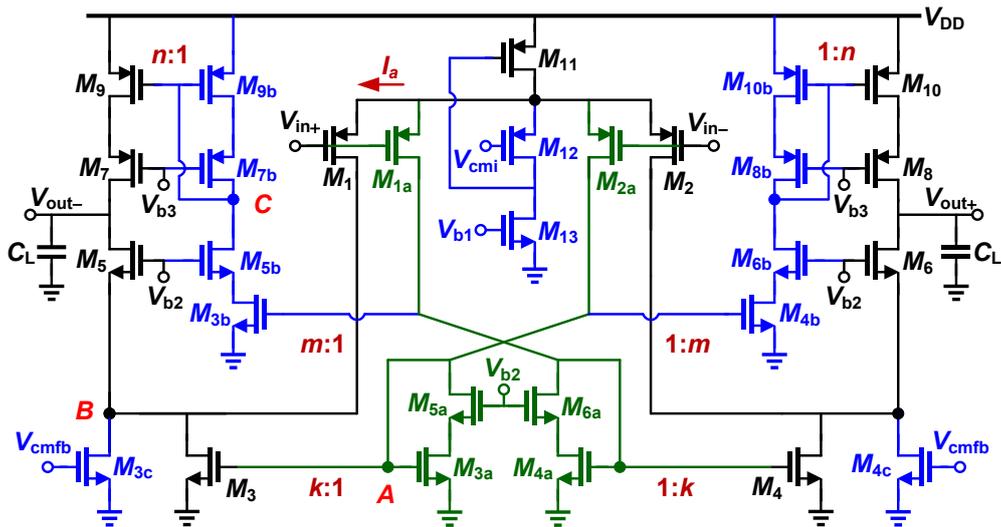


Fig. 13. Single-stage class AB fully-differential OTA [60].

input stage of the conventional folded-cascode OTA. The enhanced FCA has larger DC gain, gain bandwidth, and slew rate compared to the conventional folded-cascode amplifier, and also some improved recycling folded-cascode OTAs. A bulk-driven double recycling folded-cascode OTA has been presented in [59] for biomedical applications. The positive feedback technique with self-biased cascode transistors have been utilized to improve the small-signal transconductance, DC gain, and slew rate in low supply voltages.

5- 2- Improved Class AB Recycling Folded-Cascode OTAs

In [60], based on RFCA, a single-stage multi-path class AB OTA has been proposed, which is illustrated in Fig. 13. In this OTA, there are three different signal paths consisting of one folded-cascode and two current-mirrors. The class AB operation is realized in input stage using a flipped voltage follower cell comprising of M_{11} , M_{12} , and M_{13} transistors. Wide swing cascode current mirrors are used for improved current matching and higher DC gain. Owing to the class AB operation, the slew rate is not limited by DC bias currents,

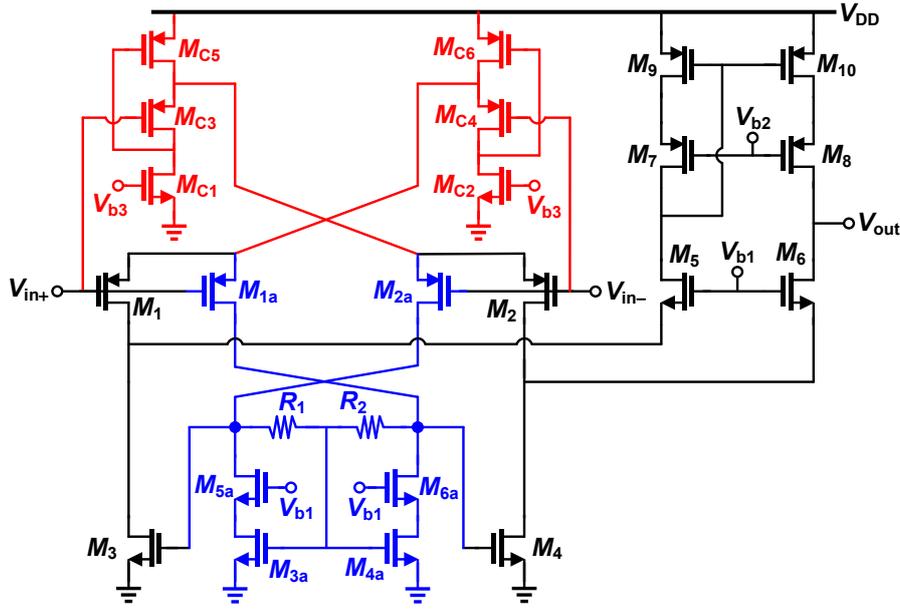


Fig. 14. Super Class AB single-ended RFCA [63].

and it depends on the input signal amplitude. The output of CMFB circuit is applied to the gate of M_{3c} and M_{4c} transistors to define the common-mode voltage of output nodes. According to the detailed analysis in [60], compared to the conventional folded-cascode OTA, the DC gain and unity-gain bandwidth are improved as:

$$A_{dc} = A_{dc,fc} \frac{(1+k+mn)}{\sqrt{2+m+mn}} \frac{R_{out}}{R_{out,fc}} \quad (15)$$

$$\omega_t = \omega_{t,fc} \frac{(1+k+mn)}{\sqrt{2+m+mn}}$$

where k , m , and n are the current mirrors ratios, as shown in Fig. 13. According to the simulation results in [60], DC gain, unity-gain bandwidth, slew rate improve about 10 dB, 215%, 650% compared to FCA, respectively.

A single-stage class AB OTA has been presented in [61] with symmetric and highly enhanced slew rate. FVF cells have been used in input pairs of RFCA to build the class AB operation in the input stage. The nonlinear current mirrors and self-biasing are utilized in output stage to boost the slew rate. The achieved slew rate is about 15 times larger than the FCA with some more power dissipation. The adaptive biasing class AB input stage using FVF cells and local Common-Mode Feedback techniques have been utilized to realize a single-ended recycling folded-cascode OTA in [62], resulting in improved small-signal transconductance and slew rate.

The proposed super class AB single-ended OTA in [63] is depicted in Fig. 14. Here, the FVF cells are employed to realize

the class AB operation in the RFCA input stage, resulting in dynamic current boosting and enhanced gain-bandwidth (GBW). The local common-mode feedback method is used at the loads of differential pair to further improve the GBW and slew rate. Its fully-differential version is shown in Fig. 15 where an additional technique that has been firstly proposed in [23], is utilized to further improve GBW and slew rate. In this technique, the gate of M_9 and M_{10} transistors is connected to the gate of M_{6c} and M_{5c} , respectively. Therefore, the small-signal current in M_{5c} and M_{6c} transistors is copied to the output nodes, and hence, DC gain, overall transconductance, and slew rate are further increased.

A super class AB single-ended RFCA has been introduced in [64] using several adaptive biasing and local common-mode feedback techniques to boost the slew rate and small-signal operation. In this OTA, two main improvements have been added to the presented OTA in [63], which is shown in Fig. 14. Two current sources have been utilized at the drain of M_{1a} and M_{2a} transistors to reduce the quiescent current of M_{3a} - M_{6a} transistors, resulting in enhanced current mirror ratios in AC operation. Moreover, the dynamic current biasing of the cascode transistors is realized with quasi floating gate techniques. Some more amplifier structures based on the quasi floating gate technique have been discussed in [65].

A fully-differential class AB RFCA with adaptive input biasing and an auxiliary amplifier to increase the DC gain has been presented in [66]. A multi-path fully-differential bulk-driven class AB OTA has been proposed in [67], where the class AB operation is realized with FVF cells at the input pairs of a RFCA. In overall, four signal paths are employed in this OTA to improve the small-signal operation and slew rate in the weak inversion region. In [68], a single-ended

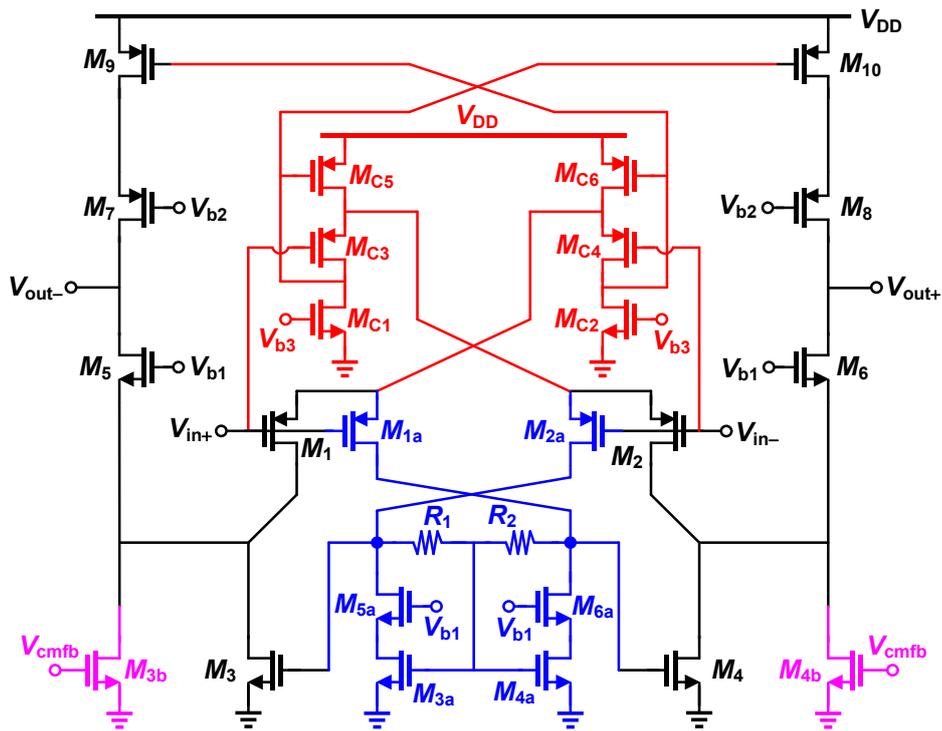


Fig. 15. Super class AB fully-differential RFCA [63].

bulk-driven class AB OTA has been suggested. In this OTA, a double recycling FCA with two FVF cells in input pairs have been utilized to build the class AB operation along with using the partial positive feedback technique.

5- 3- Two-Stage Recycling Folded-Cascode OTAs

Several two-stage OTAs using the recycling folded-cascode amplifier as the first stage have been proposed in [69-75]. A two-stage OTA has been presented in [69], where RFCA and the simple common-source amplifier are used in the first and second stages, respectively. The hybrid cascode compensation [3, 4] has been employed for the stability. Several previously reported techniques, including recycling folded-cascode, shunt current source, high-speed current mirrors, high-speed block, and high-gain block have been utilized to realize a multi-stage single-ended OTA in [70] with nested Miller compensation. Figure 16 shows the two-stage OTA structure proposed in [71], where the first stage is realized by RFCA and the second stage is a simple common-source amplifier. The Miller compensation is used for closed-loop stability. Moreover, another high-speed feedforward path is employed to provide a LHP zero for enhanced stability. This path is realized by driving the gate of transistor M_{13} with the drain voltage of M_{2a} instead of biasing the gate of M_{13} with a constant DC voltage.

Based on the current recycling technique, several two-stage class AB OTAs have been proposed in [72-75]. In [72], a two-stage class AB fully-differential OTA has been

introduced, where a recycling folded-cascode OTA with shunt current sources is used in the first stage. The class AB operation is realized in the input stage using FVF cells. The nonlinear current mirrors are employed in the second stage to boost the slew rate. The Miller compensation capacitors with null resistors are used to provide a dominant pole, which is needed for stability. A two-stage class AB fully-differential OTA has been proposed in [73], where the first stage is realized by double recycling folded-cascode OTA. Using RFCA, FVF cells, and local common-mode feedback paths, a two-stage class AB single-ended OTA has been presented in [74]. A two-stage fully-differential class AB OTA has been proposed in [75]. In this OTA, the first stage is realized by a double RFCA with a floating battery. The class AB operation is realized in the second output stage using FVF cells. The hybrid cascode compensation is used for the stability.

6- Conclusion

In this paper, several recent structural improvements of the folded-cascode amplifier and its more recent variation, which is the recycling folded-cascode OTA, have been reviewed. As it can be seen, many architectural innovations have been proposed to improve both small-signal and large-signal operations of the conventional folded-cascode amplifier. The results are promising and show considerable achievements in the design of OTAs in low-voltage and nano-meter CMOS processes.

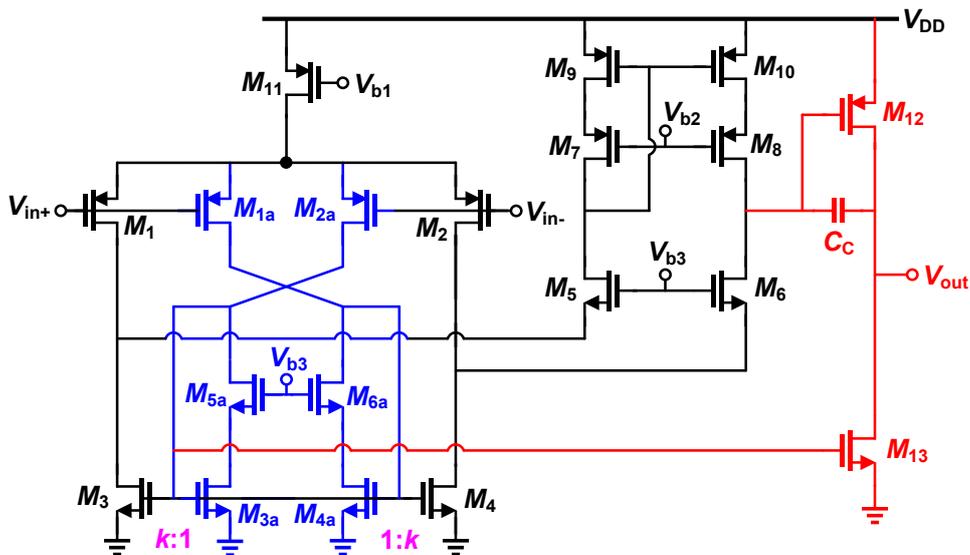


Fig. 16. Two-stage class A with RFCA as the first stage [71].

References

- [1] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Second Edition, 2012.
- [2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Second Edition, 2016.
- [3] M. Yavari and O. Shoaie, "Low-Voltage Low-Power Fast-Settling CMOS Operational Transconductance Amplifiers for Switched-Capacitor Applications," *IEE Proceedings on Circuits, Devices, and Systems*, vol. 151, no. 6, pp. 573-578, Dec. 2004.
- [4] M. Yavari, "Hybrid Cascode Compensation for Two-Stage CMOS Opamps," *IEICE Transactions on Electronics, Special Section on Analog Circuit and Device Technologies*, vol. E88-C, no. 6, pp. 1161-1165, Jun. 2005.
- [5] M. Yavari, "Active-Feedback Single Miller Capacitor Frequency Compensation Techniques for Three-Stage Amplifiers," *Journal of Circuits, Systems, and Computers, World Scientific*, vol. 19, no. 7, pp. 1381-1398, Nov. 2010.
- [6] M. Mojarad and M. Yavari, "A Low Power Four-Stage Amplifier for Driving Large Capacitive Loads," *International Journal of Circuit Theory and Applications*, vol. 42, no. 9, pp. 978-988, Sept. 2014.
- [7] S. Golabi and M. Yavari, "High-Speed Three-Stage Operational Transconductance Amplifiers for Switched-Capacitor Circuits," *Iranian Conference on Electrical Engineering (ICEE)*, Tehran, Iran, pp. 413-417, May 2014.
- [8] S. Golabi and M. Yavari, "A Three-Stage Class AB Operational Amplifier with Enhanced Slew Rate for Switched-Capacitor Circuits," *Analog Integrated Circuits and Signal Processing*, vol. 83, no. 1, pp. 111-118, Apr. 2015.
- [9] F. Alizadeh Arand and M. Yavari, "A Three-Stage NMC Operational Amplifier with Enhanced Slew Rate for Switched-Capacitor Circuits," *Analog Integrated Circuits and Signal Processing*, vol. 106, no. 3, pp. 697-706, Mar. 2021.
- [10] M. A. Mohammed and G. W. Roberts, "Generalized Relationship Between Frequency Response and Settling Time of CMOS OTAs: Toward Many-Stage Design," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 68, no. 12, pp. 4993-5006, Dec. 2021.
- [11] M. Yavari, N. Maghari, and O. Shoaie, "An Accurate Analysis of Slew-Rate for Two-Stage CMOS Opamps," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 52, no. 3, pp. 164-167, Mar. 2005.
- [12] M. Yavari, O. Shoaie, and A. Rodriguez-Vazquez, "Systematic and Optimal Design of CMOS Two-Stage Opamps with Hybrid Cascode Compensation," *Design Automation and Test in Europe, DATE*, Munich, Germany, pp. 144-149, March 2006.
- [13] M. Yavari, "A Design Procedure for CMOS Three-Stage NMC Amplifiers," *IEICE Trans. Fundamentals*, vol. E94-A, no. 2, pp. 639-645, Feb. 2011.
- [14] S. Golabi and M. Yavari, "Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits," *Analog Integrated Circuits and Signal Processing*, Springer, vol. 80, no. 2, pp. 195-208, Aug. 2014.
- [15] T.-H. Lin, C.-K. Wu, and M.-C. Tsai, "A 0.8-V 0.25-mW current-mirror OTA with 160-MHz GBW in 0.18- μm CMOS," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 54, no. 2, pp. 131-135, Feb. 2007.

- [16] S. Ali, "A power efficient gain enhancing technique for current mirror operational transconductance amplifiers," *Microelectronics Journal*, vol. 46, no. 2, pp. 183-190, Feb. 2015.
- [17] R. Póvoa, N. Lourenço, R. Martins, A. Canelas, N. Horta, and J. Goes, "Single-Stage OTA Biased by Voltage-Combiners With Enhanced Performance Using Current Starving," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 65, no. 11, pp. 1599-1603, Nov. 2018.
- [18] R. Póvoa, N. Lourenço, R. Martins, A. Canelas, N. Horta, and J. Goes, "A Folded Voltage Combiners Biased Amplifier for Low Voltage and High Energy-Efficiency Applications," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 67, no. 2, pp. 230-234, Feb. 2020.
- [19] K. Nakamura and L. R. Carley, "An enhanced fully differential folded-cascode op amp," *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp. 563-568, Apr. 1992.
- [20] G. Olivera-Romero and J. Silva-Martinez, "A folded-cascode OTA based on complementary differential pairs for HF applications," *Design of Mixed-Mode Integrated Circuits Design and Applications*, pp. 57-60, Jul. 1999.
- [21] F. Roewer and U. Kleine, "A Novel Class of Complementary Folded-Cascode Opamps for Low Voltage," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1080-1083, Aug. 2002.
- [22] J. Adut, J. Silva-Martinez, and M. Rocha-Perez, "A 10.7-MHz sixth-order SC ladder filter in 0.35- μm CMOS technology," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 53, no. 8, pp. 1625-1635, Aug. 2006.
- [23] M. Yavari and O. Shoaie, "A Novel Fully-Differential Class AB Folded-Cascode OTA," *IEICE Electron. Express*, vol. 1, no. 13, pp. 358-362, Oct. 2004.
- [24] M. Yavari and O. Shoaie, "A Novel Fully-Differential Class AB Folded-Cascode OTA for Switched-Capacitor Applications," *IEEE International Conference on Electronics, Circuits and Systems, ICECS, 2005*.
- [25] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena, and F.M. Chavero, "The Flipped Voltage Follower: a useful cell for low-voltage low-power circuit design", *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 52, no. 7, pp. 1276-1291, Jul. 2005.
- [26] J. Roh, "High-gain class AB OTA with low quiescent current," *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 2, pp. 225-228, May 2006.
- [27] M. Yavari, "A New Class AB Folded-Cascode Operational Amplifier," *IEICE Electron. Express*, vol. 6, no. 7, pp. 395-402, Apr. 2009.
- [28] A. J. Lopez-Martin, M. Pilar Garde, J. M. Algueta, C. A. de la Cruz Blas, R. G. Carvajal, and J. Ramirez-Angulo, "Enhanced Single-Stage Folded Cascode OTA Suitable for Large Capacitive Loads," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 65, no. 4, pp. 441-445, Apr. 2018.
- [29] M. Akbari, O. Hashemipour, and F. Moradi, "A High Slew Rate CMOS OTA with Dynamic Current Boosting Paths," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, May 2018.
- [30] J. Beloso-Legarra, C. A. de la Cruz-Blas, A. J. Lopez-Martin, and J. Ramirez-Angulo, "Gain-Boosted Super Class AB OTAs Based on Nested Local Feedback," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 68, no. 9, pp. 3562-3573, Sept. 2021.
- [31] F. Centurelli, P. Monsurrò, G. Parisi, P. Tommasino, and A. Trifiletti, "A Topology of Fully Differential Class-AB Symmetrical OTA With Improved CMRR," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 65, no. 11, pp. 1504-1508, Nov. 2018.
- [32] R. Assaad and J. Silva-Martinez, "Enhancing general performance of folded cascode amplifier by recycling current," *IET Electronics Letters*, vol. 43, no. 23, 8th Nov. 2007.
- [33] R. Assaad and J. Silva-Martinez, "The recycling folded-cascode: a general enhancement of the folded-cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535-2542, Sept. 2009.
- [34] R. Assaad and J. Silva-Martinez, "Recent Advances on the Design of High-Gain Wideband Operational Transconductance Amplifiers," *VLSI Design*, pp. 1-11, 2009.
- [35] R. Nagulapalli, K. Hayatleh, S. Barker, S. Zourob, and N. Yassine, "An OTA gain enhancement technique for low power biomedical applications," *Analog Integrated Circuits and Signal Processing*, vol. 95, no. 6, pp. 387-394, Jun. 2018.
- [36] M. Mohtashamnia and M. Yavari, "A Low-Power Low-Noise Neural Recording Amplifier with an Improved Recycling Telescopic-Cascode OTA," *International Journal of Electronics and Communications*, vol. 154, no. 9, pp. 1-11, 154312, Sept. 2022; Published online: Jul. 08, 2022.
- [37] Y.-L. Li, K.-F. Han, X. Tan, N. Yan, and H. Min, "Transconductance enhancement method for Operational Transconductance Amplifiers," *IET Electronics Letters*, vol. 46, no. 19, 16th Sept. 2010.
- [38] X. Zhao, H. Fang, and J. Xu, "DC gain enhancement method for recycling folded cascode amplifier in deep submicron CMOS technology," *IEICE Electron. Express*, vol. 8, no. 17, pp. 1450-1454, Sept. 2011.
- [39] Z. Yan, P.-I. Mak, and R. P. Martins, "Double recycling technique for folded-cascode OTA," *Analog Integrated Circuits and Signal Processing*, vol. 71, no. 4, pp. 137-141, Apr. 2012.
- [40] M. Akbari, "Single-stage fully recycling folded cascode OTA for switched-capacitor circuits," *Electronics Letters*, vol. 51, no. 13, pp. 977-979, 25th Jun. 2015.
- [41] T. Aghaee, S. Biabanifard, and A. Golmakani, "Gain boosting of recycling folded cascode OTA using positive feedback and introducing new input path," *Analog Integrated Circuits and Signal Processing*, vol. 47, no. 2, pp. 225-228, May 2016.
- [42] A. D. Sundararajan and S. M. Rezaul Hasan, "Quadruply Split Cross-Driven Doubly Recycled gm-Doubling Recycled Folded Cascode for Microsensor

- Instrumentation Amplifiers,” *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 63, no. 6, pp. 543-547, Jun. 2016.
- [43] X. Zhao, H. Fang, and J. Hu, “A transconductance enhanced recycling structure for folded-cascode amplifier,” *Analog Integrated Circuits and Signal Processing*, vol. 71, no. 1 pp. 259-263, Jul. 2012.
- [44] X. Zhao, H. Fang, and J. Xu, “Phase-margin enhancement technique for recycling folded cascode amplifier,” *Analog Integrated Circuits and Signal Processing*, vol. 74, no. 2, pp. 479-483, Feb. 2013.
- [45] Q. Zhang, M. Deng, and Q. Zhang, “A high DC-gain low-power current recycling amplifier in deep sub-micron CMOS technology,” *IEICE Electron. Express*, vol. 10, no. 19, pp. 1-7, Oct. 2013.
- [46] X. Zhao, H. Fang, and J. Xu, “A power-efficient improved recycling folded cascode amplifier,” *International Journal of Electronics*, vol. 100, no. 12, pp. 1660-1666, Dec. 2013.
- [47] X. Zhao, H. Fang, and J. Xu, “A Low Power Current Recycling Constant-Gm Rail-To-Rail OTA,” *Journal of Circuits, Systems, and Computers*, vol. 23, no. 2, pp. 1-12, Feb. 2014.
- [48] P.-I. Mak, M. Liu, Y. Zhao, and R. P. Martins, “Enhancing the performances of recycling folded cascode OpAmp in nanoscale CMOS through voltage supply doubling and design for reliability,” *International Journal of Circuit Theory and Applications*, vol. 42, no. 6, pp. 605-619, Jun. 2014.
- [49] M. Yavari and T. Moosazadeh, “A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits,” *Analog Integrated Circuits and Signal Processing*, Springer, vol. 79, no. 3, pp. 589-598, Jun. 2014.
- [50] U. Sonmez, H. Kulah, and T. Akin, “A $\Sigma\Delta$ micro accelerometer with 6 $\mu\text{g}/\sqrt{\text{Hz}}$ resolution and 130 dB dynamic range,” *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 11, pp. 471-485, Nov. 2014.
- [51] M. Akbari, S. Biabanifard, S. Asadi, M. C. E. Yagoub, “High performance folded cascode OTA using positive feedback and recycling structure,” *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 1, pp. 217-227, Jan. 2015.
- [52] M. Ahmed, E. Shah, F. Tang, and A. Bermak, “An Improved Recycling Folded Cascode Amplifier with Gain Boosting and Phase Margin Enhancement,” *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2473-2476, May 2015.
- [53] X. Zhao, Q. Zhang, Y. Wang, and M. Deng, “Transconductance and slew rate improvement technique for current recycling folded cascode amplifier,” *International Journal of Electronics and Communications*, vol. 70, no. 3, pp. 326-330, Mar. 2016.
- [54] M. Akbari, A. Hassanzadeh, and O. Hashemipour, “Slew rate boosting technique for an upgraded transconductance amplifier,” *Analog Integrated Circuits and Signal Processing*, vol. 88, no. 7, pp. 57-63, Jul. 2016.
- [55] S. V. Feizbakhsh, G. Yosefi, “An enhanced fast slew rate recycling folded cascode op-amp with general improvement in 180 nm CMOS process,” *International Journal of Electronics and Communications*, vol. 101, no. 3, pp. 200-217, Mar. 2019.
- [56] B. Hou, B. Zhou, X. Li, Z. Gao, Qi Wei, and R. Zhang, “An Analog Interface Circuit for Capacitive Angle Encoder Based on a Capacitance Elimination Array and Synchronous Switch Demodulation Method,” *MDPI Sensors*, vol. 19, pp. 1-12, Jul. 2019.
- [57] A. S. Khade, V. Vyas, and M. Sutaone, “A technique to enhance the transconductance of micro-power improved recycling folded cascode operational transconductance amplifier with reasonable phase margin,” *International Journal of Electronics and Communications*, vol. 108, no. 8, pp. 148-157, Aug. 2019.
- [58] Y. Wang, Q. Zhang, S. S. Lu, X. Zhao, H. Trinh, and P. Shi, “A Robust Local Positive Feedback Based Performance Enhancement Strategy for Non-Recycling Folded Cascode OTA,” *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 67, no. 9, pp. 2897-2908, Sept. 2020.
- [59] A. Ghaemnia and O. Hashemipour, “An ultra-low power high gain CMOS OTA for biomedical applications,” *Analog Integrated Circuits and Signal Processing*, vol. 99, no. 6, pp. 529-537, Jun. 2019.
- [60] M. Yavari, “Single-stage class AB operational amplifier for SC circuits,” *IET Electronics Letters*, vol. 46, no.14, pp. 977-979, 8th July 2010.
- [61] X. Zhao, Y. Wang, D. Jia, and L. Dong, “Ultra-high current efficiency single-stage class-AB OTA with completely symmetric slew rate,” *International Journal of Electronics and Communications*, vol. 87, no. 4, pp. 65-69, Apr. 2018.
- [62] X. Zhao, Y. Wang, and L. Dong, “Super current recycling folded cascode amplifier with ultra-high current efficiency,” *Integration, the VLSI Journal*, vol. 62, no. 6, pp. 322-328, Jun. 2018.
- [63] M. Pilar Garde, A. Lopez-Martin, R. Gonzalez Carvajal, and J. Ramirez-Angulo, “Super Class-AB Recycling Folded Cascode OTA,” *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2614-2623, Sept. 2018.
- [64] J. M. Algueta-Miguel, A. Lopez-Martin, M. Pilar Garde, C. A. De la Cruz, and J. Ramirez-Angulo, “ ± 0.5 V 15 μW Recycling Folded Cascode Amplifier With 34767 MHz·pF/mA FOM,” *IEEE Solid-State Circuits Letters*, vol. 1, no. 7, pp. 170-173, Jul. 2018.
- [65] A. Lopez-Martin, M. Pilar Garde, J. M. Algueta-Miguel, J. Beloso-Legarra, R. G. Carvajal, and J. Ramirez-Angulo, “Energy-Efficient Amplifiers Based on Quasi-Floating Gate Techniques,” *Applied Sciences*, vol. 11, pp. 1-19, Apr. 2021.
- [66] X. Lv, X. Zhao, Y. Wang, L. Dong, Y. Xin, and L. Yu, “A low-power second-order sigma-delta modulator for MEMS digital geophones,” *International Journal of Electronics and Communications*, vol. 119, no. 5, pp. 1-9, May 2020.
- [67] Q. Zhang, Y. Wang, X. Zhao, and L. Dong, “Single-stage multipath class-AB bulk-driven OTA with enhanced power efficiency,” *International Journal of Electronics*

- and *Communications*, vol. 107, no. 7, pp. 39-48, Jul. 2019.
- [68] N. Deo, T. Sharan and T. Dubey, "Subthreshold biased enhanced bulk-driven double recycling current mirror OTA," *Analog Integrated Circuits and Signal Processing*, vol. 105, no. 11, pp. 229-242, Nov. 2020.
- [69] B. Wen, Q. Zhang, X. Zhao, X. Lv, and Y. Wang, "Trade-offs among power consumption and other design parameters of two-stage recycling folded cascode OTA that using embedded cascode current buffer compensation technology," *Integration, the VLSI Journal*, vol. 68, no. 9, pp. 62-70, Sept. 2019.
- [70] P.-Y. Kuo and S.-D. Tsai, "An Enhanced Scheme of Multi-Stage Amplifier With High-Speed High-Gain Blocks and Recycling Frequency Cascode Circuitry to Improve Gain-Bandwidth and Slew Rate," *IEEE Access*, vol. 7, pp. 130820-131829, Sept. 2019.
- [71] Y. Xin, X. Zhao, B. Wen, L. Dong, and X. Lv, "A High Current Efficiency Two-Stage Amplifier With Inner Feedforward Path Compensation Technique," *IEEE Access*, vol. 8, pp. 22664-22671, Feb. 2020.
- [72] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, and K.-Y. Lee, "98-dB Gain Class-AB OTA With 100 pF Load Capacitor in 180-nm Digital CMOS Process," *IEEE Access*, vol. 7, pp. 17772-17779, Feb. 2019.
- [73] S. Banagozar and M. Yargholi, "Ultra-low power two-stage class-AB recycling double folded cascode OTA," *International Journal of Electronics and Communications*, vol. 110, no. 10, pp. 1-12, Oct. 2019.
- [74] A. Yen and B. J. Blalock, "A High Slew Rate, Low Power, Compact Operational Amplifier Based on the Super-Class AB Recycling Folded Cascode," *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 9-12, Aug. 2020.
- [75] C. Park, Y. A. Tavares, J. Lee, J. Wo, and M. Lee, "5th-Order Continuous-Time Low-Pass Filter Achieving 56 MHz Bandwidth 30.5 dBm IIP3 With a Novel Low-Distortion Amplifier," *IEEE Transactions on Circuits and Systems—II: Express Briefs*, vol. 68, no. 6, pp. 1768-1772, Jun. 2021.

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