A Low Power Low Voltage Rail to Rail Constant gm Differential Amplifier with 150 dB CMRR and Enhanced Frequency Performance

Leila Safari[i] and Seyed Javad Azhari[ii*]

ABSTRACT

This paper proposes a low voltage (±0.55V supply voltage) low power (44.65µW) high common mode rejection ratio (CMRR) differential amplifier (d.a.) with rail to rail input common mode range (ICMR), constant transconductance (gm) and enhanced frequency performance. Its high performance is obtained using a simple negative averaging method so that it cancels out the common mode input signals at the same input terminals while preserving high frequency operation. The principle of operation, small signal analysis and the formula of its most important parameters are explained and derived. Simulation results with HSPICE using TSMC 0.18µm CMOS are presented showing rail to rail operation, CMRR of 150dB, voltage gain of 31.6dB, gain bandwidth of 95.8 MHz and input referred noise of 100.64nv/√Hz. Compared to conventional amplifier ones those are 94.4dB , 3.4dB, 1.62 times and 1.72 times better, respectively. The CMRR corner case simulation results are also provided showing from 52.1dB to 74.6dB improvement over conventional one.

KEYWORDS

High CMRR Differential Amplifier, Low Voltage, Low Power, Rail to Rail, Quasi Floating Gate

1. INTRODUCTION

In recent years downscaling trend of integrated circuit technology in general and increase of portable electronics and solar powered systems in particular have considerably increased the demand for low supply circuits and systems [1]-[3]. It is predicted that in the near future, supply voltage of analog and mixed mode circuits will be less than |VTHP|+VTHN(in which VTHP and VTHN are the threshold voltages of PMOS and NMOS transistors respectively)[4].

Unfavorably supply voltage reduction and transistor size scaling down, impose serious challenges on the design of analog integrated circuits. Transistors high threshold voltages (threshold voltage reduction is less than that of supply voltage), low intrinsic gain and low output impedance are some of the serious analog integrated circuit design contrasts in modern CMOS technologies [5]-[6].

Differential amplifiers as the input stage of such analog signal processors as operational amplifiers [7]-[8], operational transconductance amplifiers (OTA), filters and the like have faced with difficulties in low voltage supplies, too. The required voltage to keep all transistors of a differential amplifier in saturation has become a significant fraction of the allowed supply voltages in modern deep sub micron CMOS technology which results in a reduced room for common mode input signals. As a result, differential amplifiers greatly suffer from reduction of both input common mode range (ICMR) and common mode rejection ratio (CMRR) in modern CMOS technologies. In deep submicron technologies output impedance of tail current source is low (due to reduced output impedance of transistors) causing tail current to vary as the common mode signal varies resulting in a poor CMRR. This is why cascode tail current sources are used for high values of CMRR [9] which in turn increases the required supply voltage to values incompatible with today's CMOS technology. Tail current source variation with common mode signals also means a non constant transconductance (gm) for differential amplifier. A large variation in gm introduces signal distortion and creates difficulty in frequency compensation of Op-amps [10], [11]. As a result, a nearly constant gm over the rail to rail ICMR is essential for differential amplifiers. Some high output impedance tail current sources to achieve higher CMRR and reducing

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tail current variations have been reported in [12]-[14]. Unfavorably these tail current sources result in a reduced ICMR in deep submicron CMOS technologies, the same problem which is noticed in [15] concerning [13].

Traditional approach for obtaining rail to rail ICMR is using complementary differential pairs (CDP) [16]-[18]. Unfavorably complex circuitry is usually required in these circuits to ensure a constant gm which increases power consumption. On the other hand, there is a dead zone for input CM voltages in the middle band of the supply voltages where the input voltage is able to turn on none of the differential pairs [19].

Multiple input floating gate (MIFG) transistors provide a simple way to design low voltage and low power rail to rail differential amplifiers. A MIFG based differential amplifier is shown in Fig.1. In this architecture input signals are attenuated by capacitive dividers before processing by differential amplifier [20]-[22]. The input signals are attenuated enough to always remain in the ICMR of the amplifier. The capacitor ratio is usually set around five which results an attenuation of six [21]. Although attenuation of input signals extends ICMR, it also results in an effective reduction in differential amplifier transconductance, dynamic range and gain bandwidth product and an increase in input referred noise. On the other hand, MIFG based differential amplifier exhibit a non constant gm (with deviation of 3%) due to the output impedance of tail current source as commented in [23]. However, gm variation is reduced in [15], [23] employing dynamic bias approach. In [23] tail current source variation is reduced in a way that any common mode voltage variation on the tail current source is sensed and compensated at the differential amplifier inputs which resulted in a CMRR of 88dB and a gm variation of ±0.35% for rail to rail ICMR. Major drawback of this work is its high power dissipation because of the voltage amplifier employed in the feedback loop. The same method is implemented in [15] with reduced number of elements and less complexity which resulted in a CMRR of 108dB and a nearly constant gm. Unfavorably its gain bandwidth is reduced from 61MHz in conventional one to 27MHz. The design procedure is rather complicated in [15], [23] because negative feedback stability problems have to be considered. Dynamic biasing method used in [24] to relax the capacitor ratios and reduce gain bandwidth degradation effect has resulted in a CMRR of only 88dB and there is no report on gm variation.

Unfortunately, MIFG based circuits suffer from the large DC offsets produced by trapped charge on the floating gates which need expensive processing steps, special layout techniques[25] or quasi floating gate(QFG) transistors[1] to be removed. In QFG approach, the gate is not truly floating, but weakly connected to a DC voltage through a very large valued resistor so trapped charges are removed and the DC operating point of the gate is accurately set [1]. Fig.2 shows a QFG based differential amplifier [26].The resistors have to be large in order to allow the gate terminal to perform as a pseudo floating gate terminal. Some possible implementations of large resistors can be found in [27]. In order to allow rail-to-rail operation, input signals are attenuated by means of capacitive dividers implemented with QFGs input capacitors. To do so, as shown in Fig.2, one pair of inputs (Cm) are connected to ground while other input terminals (C1-C2) are assigned to input signals. The capacitors connected to ground need to be larger than the capacitors connected to input signals. In [26] the capacitor connected to ground was made two times larger than those connected to input sources(i.e. Cm=2C1=2C2) which has resulted in attenuation of three for input signals which also means a degradation factor of three in transconductance, gain bandwidth product and an increase in input referred noise by the same amount. Due to the low output impedance of tail current source, CMRR is also poor and gm is not constant.

In this paper, a new QFG based low power low voltage differential amplifier with rail-to-rail operation, very high CMRR and constant gm is introduced. A novel negative averaging method is used to suppress the common mode signals right at the differential amplifier input ports which allow a gain bandwidth attenuation factor of only two, higher CMRR, rail to rail operation and constant gm. Other performance parameters such as power supply rejection ratio and input referred noise are also improved compared to conventional QFG based d.a.. The proposed structure is very compact and power efficient. This paper is arranged as follows. In Section II the proposed circuit is explained. The simulation results are presented in Section III and finally Section IV concludes this paper.

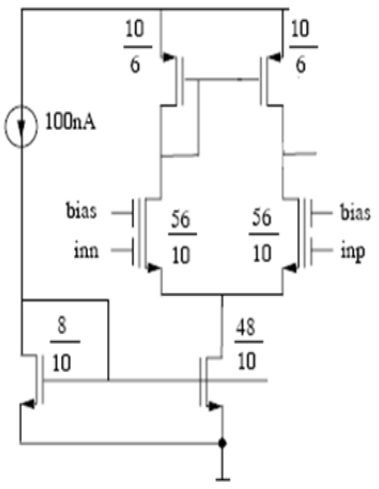


Figure 1: MIFG based differential amplifier [19].

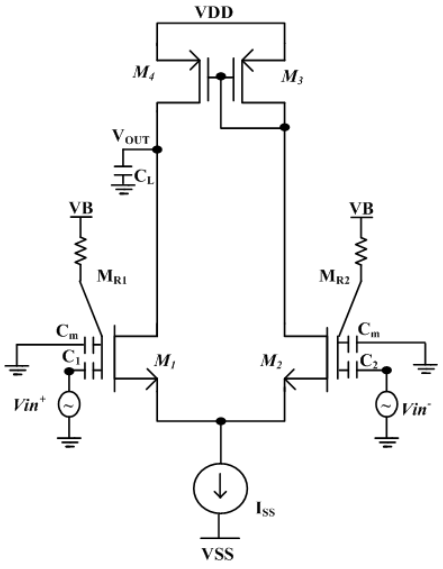


Figure 2: QFG based differential amplifier [26].

2. THE PROPOSED DIFFERENTIAL AMPLIFIER

The conceptual schematic of the proposed idea is shown in Fig.3 in which M1-M2 are d.a. input transistors, M3-M4 are load transistors and MR1-MR2 are large value resistors connected to VB to provide proper bias voltage for d.a. transistors and remove trapped charges on M1-M2 floating gates. Input signals are applied via C1-C2 terminals and their negative average $(-0.5\times(Vin^{+}+Vin^{-}))$ are applied via Cm to the input ports of differential amplifier. Assuming C1-C2 and Cm are larger than parasitic capacitors of M1-M2, small signal floating gate voltages of M1-M2 will be weighted the sum of two inputs as stated in (1) and (2):

$$V_{FG1}=Vin^{+}\times\frac{C_1}{C_1+Cm}-0.5\times(Vin^{-}+Vin^{+})\times\frac{Cm}{C_1+Cm} \quad (1)$$

$$V_{FG2}=Vin^{-}\times\frac{C_1}{C_1+Cm}-0.5\times(Vin^{-}+Vin^{+})\times\frac{Cm}{C_1+Cm} \quad (2)$$

Assuming C1=C2=C, equations (1) and (2) can be simplified to:

$$V_{FG1}=\frac{C}{C+Cm}\times\left[\frac{Vin^{+}-Vin^{-}}{2}\right]=\frac{1}{2}\times\left[\frac{Vin^{+}-Vin^{-}}{2}\right] \quad (3)$$

$$V_{FG2}=-\frac{C}{C+Cm}\times\left[\frac{Vin^{+}-Vin^{-}}{2}\right]=-\frac{1}{2}\times\left[\frac{Vin^{+}-Vin^{-}}{2}\right] \quad (4)$$

Arranging input voltages in terms of common mode $(V_{cm}=\frac{Vin^{+}+Vin^{-}}{2})$ and differential mode $(V_{dm}=Vin^{+}-Vin^{-})$ components as:

$$Vin^{+}=\frac{V_{dm}}{2}+V_{cm} \quad (5)$$

$$Vin^{-}=-\frac{V_{dm}}{2}+V_{cm} \quad (6)$$

And inserting (5) and (6) into (3) and (4) yields M1-M2 gate voltages as:

$$V_{FG1}=\frac{C}{C+C_m}\times\frac{V_{dm}}{2}=\frac{1}{2}\times\frac{V_{dm}}{2} \quad (7)$$

$$V_{FG2}=-\frac{C}{C+C_m}\times\frac{V_{dm}}{2}=-\frac{1}{2}\times\frac{V_{dm}}{2} \quad (8)$$

As (7) and (8) imply, only differential mode components of input voltages are applied to M1-M2 gates and common mode components are easily canceled out with no need to large value attenuating capacitors or complicated negative feedbacks but just due to usage of the proposed method. This means a higher CMRR and constant gm for the proposed d.a. along with rail to rail operation. The reason is that, due to cancelation of input common mode signals at the differential amplifier inputs, no common mode is sensed with tail current source resulting in a constant tail current with no need to a high output impedance tail current source.

Negative average of input signals can be simply implemented by three input amplifier shown in Fig.4-a in which input signals are applied via C3-C4 inputs while C5 input is grounded. Grounding C5 attenuates input signals extending ICMR of the amplifier of Fig.4. Note that attenuation in the negative averaging circuit of Fig.4 does not have any effect on the main differential amplifier gain and gain band width product. Biasing of negative averaging circuit is provided by large value resistors of MR3 and MR4. Due to large signal swing at the output of this block, two series connected resistors are used in this circuit to avoid forward biasing the reverse biased PN junctions implementing large value resistors [27]. All large value resistors are implemented using PMOS transistors in cutoff due to their gates connected to VDD.

Small signal model of Fig.4-a is shown in Fig.4-b. Since the low cut off frequency, fL, of Fig.4-a is in the range of sub hertz [26], large value resistors are ignored in the small signal model which is used for regularly used frequencies. From Fig.4-b it is understood:

$$ro=ro_5\|ro_6 \quad (9)$$

$$Co=C_{ds6}+C_{db6}+C_{ds5}+C_{db5}+C_{sbMR4} \quad (10)$$

$$C_3=C_4=C' \quad (11)$$

Writing KCL at nodes (1) and (2) in Fig. 4-b gives:

$$\frac{V_f}{r_o}+V_f C_o S+gm_5V_{gs5}=(V_{gs5}-V_f)\times(C_{gd5}+C_6)\times S \quad (12\text{-a})$$

$$(Vin^{+}+Vin^{-})\times C'\times S-2\times V_{gs5}\times C'\times S$$
$$=V_{gs5}\times(C_5+C_{gs5})\times S+(V_{gs5}-V_f)\times(C_6+C_{gd5})\times S \quad (12\text{-b})$$

$$\rightarrow \frac{V_f}{(Vin^+ + Vin^-)} \approx -\frac{1}{1+\frac{S}{P_1}} \times \frac{C' \times g_{m5} \times r_o}{2C' + C_5 + C_{gs5} + C_{gd5} + C_6 + g_{m5}.r_o.(C_6 + C_{gd5})} = \frac{-K}{1+\frac{S}{P_1}} \quad (13)$$

Or:

$$V_f \approx \frac{-K}{1+\frac{S}{P_1}} \times (Vin^+ + Vin^-) \quad (13\text{-a})$$

Where:

$$K = \frac{C' \times g_{m5} \times r_o}{2C' + C_5 + C_{gs5} + C_{gd5} + C_6} \approx \frac{C'.g_{m5}.r_o}{2C' + C_5 + C_6} \quad (13\text{-b})$$

$$P_1 = [\frac{2C' + C_5}{g_{m5}}]^{-1} \quad (13\text{-c})$$

In order to produce negative average of input signals, K in (13-b) should be set to 0.5.

Complete schematic of the proposed high CMRR, high frequency and rail to rail d.a. is shown in Fig.5 in which A1 is the main d.a. and A2 is the negative averaging block.

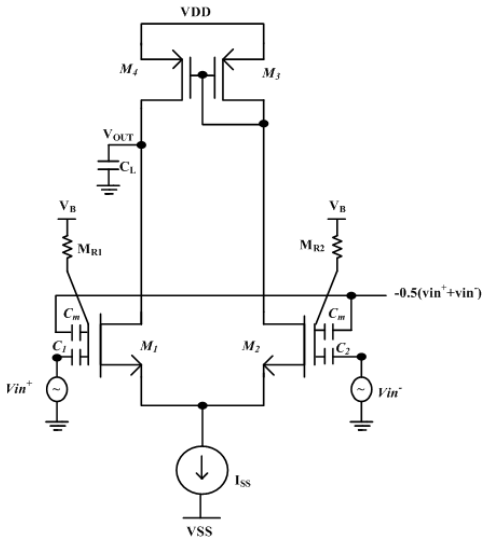


Figure :3 The conceptual schematic of the proposed idea.

The CMRR of the proposed d.a. can be calculated from (14) in which VFG_{dm} and VFG_{cm} are differential mode and common mode gate voltages of M1-M2 respectively, Rss is the output resistance of tail current source, $gm_{1,2}$ is the transconductance of M1-M2 and λ is the current gain of M3-M4 load current mirror.

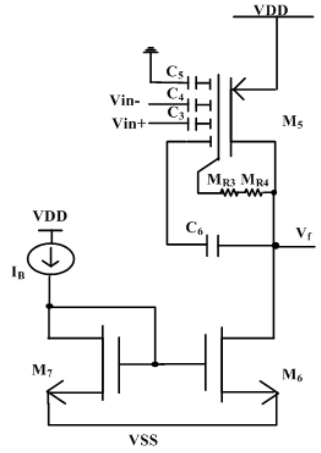
$$CMRR = \frac{VFG_{dm}}{VFG_{cm}} \times \frac{(1+\frac{S}{P_{ss}})}{1+2.gm_{1,2}.R_{ss}} \times \frac{(1+\lambda)}{(1-\lambda)} \quad (14)$$

where: $P_{ss} = (2.\pi.R_{ss}.C_{ss})^{-1}$ and C_{ss} is the output capacitance of tail current source.

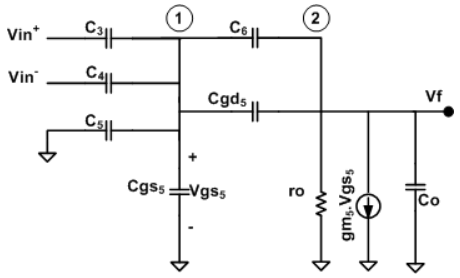
The ac gate voltages of M1-M2 in Fig.5 are:

$$V_{FG2} = Vin^- \times \frac{C}{C+Cm} + V_f \times \frac{Cm}{C+Cm} \quad (15)$$

$$V_{FG1} = Vin^+ \times \frac{C}{C+Cm} + V_f \times \frac{Cm}{C+Cm} \quad (16)$$



(a)



(b)

Figure 4: Negative averaging block (a) Schematic (b) Small signal equivalent circuit.

Inserting V_f from (13) into (15) and (16) and considering a common mode voltage of V_{CM} ($Vin^+ = Vin^- = V_{CM}$) at inputs, the common mode gate voltage of M1-M2 becomes as:

$$(V_{FG1})_{CM} = (V_{FG2})_{CM} = V_{CM} \times (1-2K) \times \frac{(1-\frac{S}{(1-2K)P_4})}{(1+\frac{S}{P_1})} \quad (17)$$

It can be seen from (17) that common mode gate voltages of M1-M2 in Fig.5 will be suppressed if the K factor is set as close as possible to 0.5. Such resulted zero common mode input voltage also provides rail to rail operation and constant gm for the proposed differential amplifier.

In the case of differential mode inputs (Vin^+=-Vin^- =V_{dm}), V_f approaches zero according to (13-a). Then using (1) and (2), the differential mode gate voltage of M1-M2 becomes:

$$(V_{FG2})_{dm} = V_{dm} \times \frac{C_2}{C_2 + C_m} + V_f \times \frac{C_m}{C_2 + C_m} =$$

$$V_{dm} \times \frac{C_2}{C_2 + C_m} + 0 \times \frac{C_m}{C_2 + C_m} = V_{dm} \times \frac{C_2}{C_2 + C_m} = \frac{V_{dm}}{2} \quad (18)$$

In the same way $(V_{FG1})_{dm}$ is found as:

$$(V_{FG1})_{dm} = \frac{V_{dm}}{2} \quad (19)$$

Using (17)-(19), CMRR of the proposed d.a. of Fig.5 is given by:

$$CMRR = \frac{1}{2(1-2K)} \times \frac{(1+\frac{S}{P_{ss}})}{(1+2.gm_{1,2}.R_{ss})} \times \frac{(1+\lambda)}{(1-\lambda)} \times \frac{(1-\frac{S}{(1-2K)P_1})}{(1+\frac{S}{P_1})} \quad (20)$$

The CMRR boosting of the proposed d.a. can be clarified by comparing (20) with the CMRR of the conventional d.a. given in (21) (which is represented by $CMRR_c$):

$$CMRR_c = \frac{(1+\frac{S}{P_{ss}})}{(1+2.gm_{1,2}.R_{ss})} \times \frac{(1+\lambda)}{(1-\lambda)} \quad (21)$$

In the conventional d.a. of Fig.2, the second inputs (Cm) of M2 and M4 are tied to ground to provide proper attenuation for rail to rail operation. This attenuation also takes place for differential mode signals. Hence common mode attenuation with capacitive dividers does not result in any increase in CMRR. While in the proposed method, common mode inputs are extremely canceled out at the gates of M1-M2 as is seen from (17) and the differential mode input signals are transferred to the differential amplifier input transistors by an attenuation of only two (as is seen from (18) and (19)). Consequently, CMRR in the proposed differential amplifier will be considerably boosted as is given by (20). The denominator of (20) can be close to zero by making K as close as possible to 0.5. A near zero denominator for (20) results in an extremely high CMRR for the proposed differential amplifier. The condition K=0.5 can be simply accomplished by proper sizing of M5-M6 and C5-C6 values in (13-a).

It is worth noting that unlike the methods used in [15, 23], there is no negative feedback in the proposed scheme. Consequently, it is not necessary to consider the circuit stability and design procedure is very simple and straight forward. On the other hand, high CMRR and rail to rail operation with constant gm for the proposed d.a. is provided by a very simple method needing the small number of components to satisfy the low voltage low power requirements.

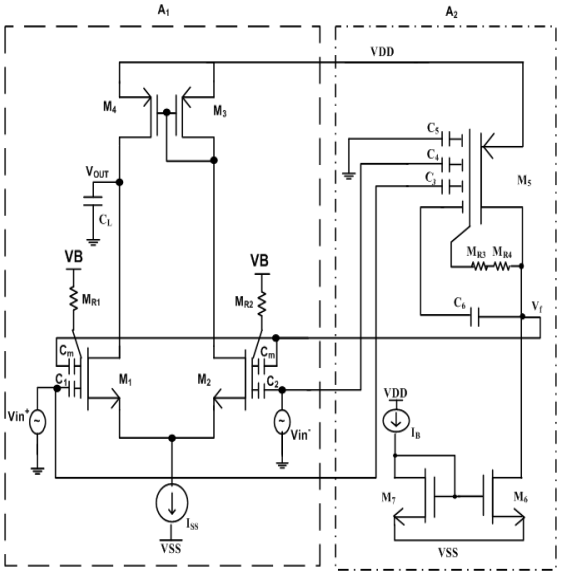


Figure 5: Schematic of the proposed differential amplifier.

The proposed scheme can also be implemented in fully differential configuration as is shown in Fig.6. This arrangement can then considerably increase such parameters as CMRR, PSRR and differential gain of the block. Most favorably those parameters could be increased over and over by cascading the fully differential configuration so many times that maintain the required values, of course within the allowable limits of consumed power.

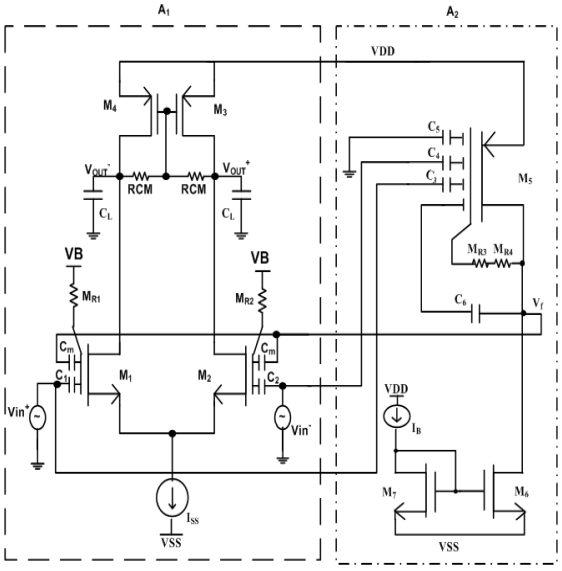


Figure 6: Proposed d.a. in fully differential configuration.

3. SIMULATION RESULTS

The circuits of Fig. 5 and Fig.2 to which we will refer as proposed and conventional differential amplifiers respectively, were designed and simulated in 0.18µm TSMC CMOS technology with nominal threshold voltages of 0.43V and -0.45V for NMOS and PMOS

transistors respectively. The transistors dimensions, bias settings and elements values are summarized in Tables 1, 2 and 3 respectively. It is worth noting that since the used capacitors are small, they can be implemented as metal-metal or metal-poly capacitors in mainstream digital CMOS technology without the need of a second poly layer [24]. As a result, we used 0.18µm TSMC CMOS technology for design and simulation. The used aspect ratios for transistors implementing large value resistors are also given in table 1. Observe that current generators were implemented through simple current mirrors with aspect ratios of 3µm/0.5µm.

Fig.7 compares the gate voltages of input transistors of the proposed and conventional differential amplifiers due to applied sinusoidal common mode inputs of 0.2v peak to peak. It demonstrates the great strength of the proposed method in suppression of the common mode voltages at the gate terminals of the proposed d.a. while the input transistors' gate terminals preserve their DC bias voltage of 0.1v. These results are in good agreement with (17). DC bias voltage of 0.1v is provided by large value resistors connected to VB.

In Fig.8 tail current variation versus rail to rail common mode inputs are compared between proposed and conventional differential amplifiers. As is shown, tail current source in the proposed d.a. maintains an approximately constant current over -0.45v to 0.45v input common mode range while the conventional d.a. has a deviation of 16.66% in the tail current source in this range. Conventional d.a. has a large deviation of 21% and 3.76% for the common mode voltages equal to the negative and positive rails respectively. While in the proposed d.a. those are only 2.5% and 0.75% which are mainly due to the fact that in the related region, gain of negative averaging block deviates from 0.5 causing some variation in tail current source.

Although Fig.8 reflects the related information of the gm of the discussed differential amplifiers (since it is directly proportional to tail current) however, gm variations versus input rail to rail common mode signal is also considered which is shown in Fig.9. These results show that when input common signal varies from negative supply value to the value of positive one, gm of proposed d.a. varies from 2% to 0.62% , respectively, while these variations are from 15.72% to 2.56%, respectively, for conventional d.a. Comparing these two sets of results proves the rather harmony between gm and tail current as well as the great superiority of the proposed d.a. over the conventional one in providing a constant gm versus a rail to rail input common signal.

CMRR behavior of the circuits is illustrated in Fig. 10 which shows a low frequency value of 150 and 55.6dB for the proposed and conventional differential amplifiers respectively. The proposed solution provides an improvement of 94.4 dB for the proposed d.a over conventional one. Figure 10 is practically a quantitative interpretation of the fact shown in Figure 7. Although these two sets of results seem enough to prove the superiority of the proposed d.a. over the conventional one in terms of both CMRR and rail to rail ICMR, to further investigate the issues we also tried the method used in [23] as follows. A common-mode 50-Hz rail to rail triangular signal (whose amplitude is increased to rail-to-rail, as is shown in Fig.11-a) mixed with a 2 mV peak-to-peak 200Hz sinusoidal differential one (Fig.11-b) are applied to both proposed d.a. and conventional one. The resulted output voltages (Fig.11-c) show that the output of the proposed d.a. remains unchanged regardless of the large amplitude of common-mode signal (ranged from -0.55v to 0.55v) while the output of the conventional d.a. has large variations with common mode level so that as the input common signal amplitude increases up the output combined signal amplitude reduces down point by point.

The gain frequency responses of the proposed and conventional differential amplifiers are shown in Fig. 12 which demonstrate improved low frequency gain and gain-bandwidth product for the proposed differential amplifier. Gain bandwidth of the proposed d.a. is 95.8Mhz while that of the conventional one is only 58.9Mhz which shows an improvement of 1.62 times for the former one.

Power supply rejection ratio (PSRR) simulation results are shown in Fig.13. As can be seen, PSRR+ in the proposed d.a. is 31.6 dB which is 3.4dB higher than that of the conventional one with superior frequency performance. PSRR- is 58dB and 49.2dB in the proposed and conventional differential amplifiers respectively which shows an improved value of 8.8dB for the proposed one.

The input-referred voltage noise at 100 KHz was also evaluated showed values of 173.57nV/√Hz for the conventional d.a. and 100.64nV /√Hz for the proposed one. It exhibits a rather improved noise performance for the proposed d.a..

The proposed d.a. was arranged in unity gain configuration with a load of 1pF. Fig.14 shows the short circuit input-output transfer characteristic and the transient response to a 0.3V input step.

To study the effect of technology process (mismatches and other non-idealities) on the CMRR we also executed the corner case simulations the results of which are summarized in Table 4. As can be deduced from results, the CMRR of the proposed d.a. remains from 52.1 dB to 74.6dB higher than the CMRR of conventional one.

To investigate CMRR variation with mismatches Monte Carlo simulation was carried out by considering 3% mismatch in threshold voltage, W, L and Tox of transistors in 100 runs. The resulted CMRR variation for both proposed and conventional differential amplifiers

are shown in Fig.15. The average value of CMRR is 110.4445dB and 49.47dB for the proposed and conventional differential amplifiers respectively. The Monte Carlo simulation is also carried out by considering 5% mismatch which showed CMRR average value of 93.70dB and 46.92dB for the proposed and conventional differential amplifiers respectively. As can be seen, the average value of CMRR in the proposed d.a. is 60.97dB and 46.78dB larger than the one for conventional d.a. in the case of 3% and 5% mismatch, respectively.

The performance characteristics of the proposed differential amplifier and the conventional one in 0.18µm technology are summarized in Table 5 which prove promising performance of the proposed differential amplifier over conventional one in terms of CMRR, gain bandwidth product, PSRR, etc. A comparison of this work to some other advanced works on this topic is presented in Table 6. The results in table 6 show that besides the lower output impedance of the tail current source of the proposed d.a. compared to those of other works (due to related limitations of 0.18µm technology compared to those of 0.5µm technology) it has superior CMRR over all of other referenced works which proves strong effectiveness of the proposed structure in this respect. On the other hand, structures reported in [15, 23], have larger capacitors at the differential amplifier inputs compared to proposed d.a.. As a result, these structures need a double poly CMOS process while the proposed d.a. can be implemented in the less costly digital CMOS process and provides much larger CMRR compared to those works.

TABLE .1
TRANSISTORS ASPECT RATIOS

		Proposed	Conventional
Transistor		Aspect Ratio	Aspect Ratio
M1		7µm/2µm	7µm/2µm
M2		7µm/2µm	7µm/2µm
M3		9µm/0.8µm	9µm/0.8µm
M4		9µm/0.8µm	9µm/0.8µm
M5		1.1µm/0.3µm	NA
M6		1µm/0.3µm	NA
M7		1µm/0.3µm	NA
Resistors	MR1-MR2	0.5µm/0.5µm	0.5µm/0.5µm
	MR3-MR4	0.5µm/0.5µm	NA

TABLE .2
BIAS SETTINGS.

Parameter	Value
VDD	0.55V
VSS	-0.55V
VB	0.2V
IB	1 µA
Iss	20µA

TABLE .3
ELEMENT VALUES.

Proposed d.a.		Conventional d.a.	
Element	Value	Element	Value
C1- C4	100f	C1- C2	100f
Cm	100f	Cm	300f
C5	500f	-	-
C6	171.2f	-	-
CL	100f	CL	100f

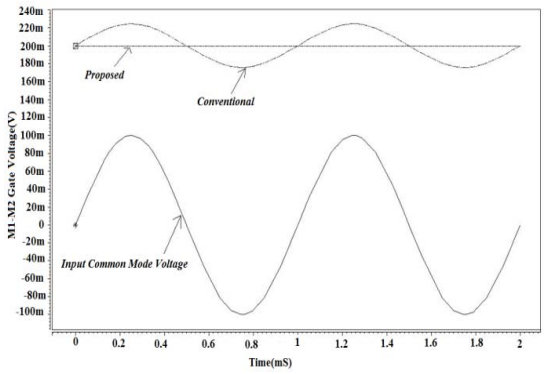


Figure 7: M1-M2 gate voltages (top curve) resulted by a 0.2Vpp sinusoidal common mode input (bottom curve) in the proposed and conventional differential amplifiers.

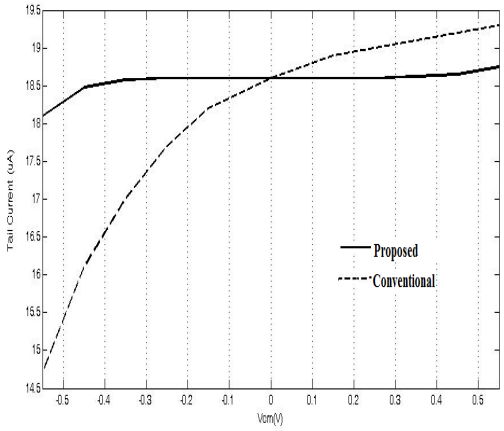


Figure 8: Tail current variation versus common mode input voltage.

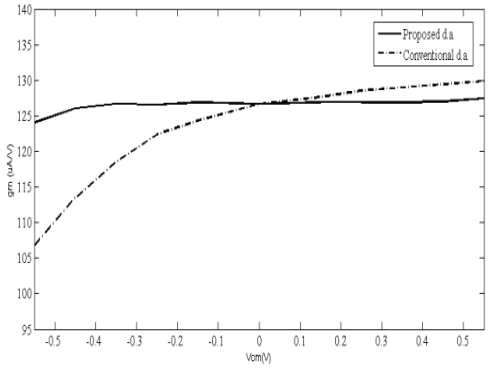


Figure 9: Gm variation versus common mode input voltage.

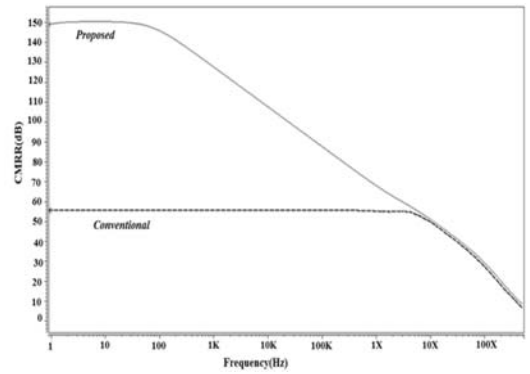
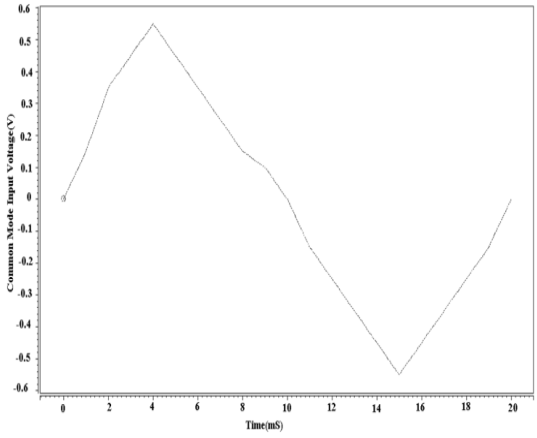
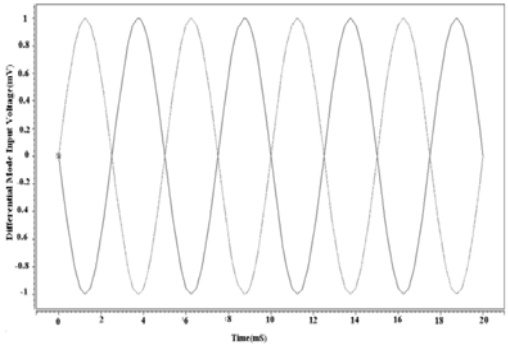


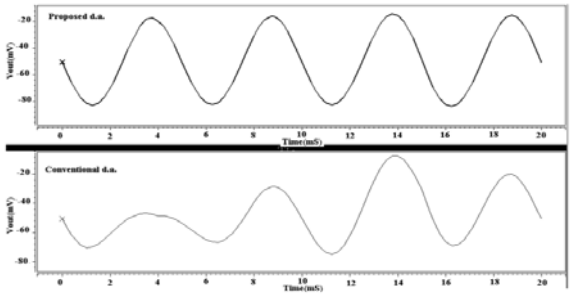
Figure 10: CMRR frequency performances of the proposed and conventional differential amplifiers.



(a)



(b)



(c)

Figure 11.(a)Input common mode signal, and (b) differential mode one applied to both proposed d.a. and conventional one . (c) the resulted output for the proposed and conventional differential amplifiers.

TABLE 4
CMRR CORNER CASE SIMULATION RESULTS FOR THE PROPOSED AND CONVENTIONAL DIFFERENTIAL AMPLIFIERS.

	TT	Corner cases(dB)			
		FF	SS	SF	FS
Proposed (dB)	150	113	103	123	113
Conventional(dB)	55.6	60.9	46	48.4	47.5

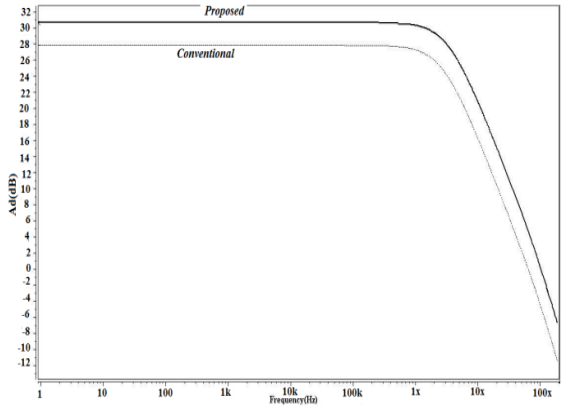
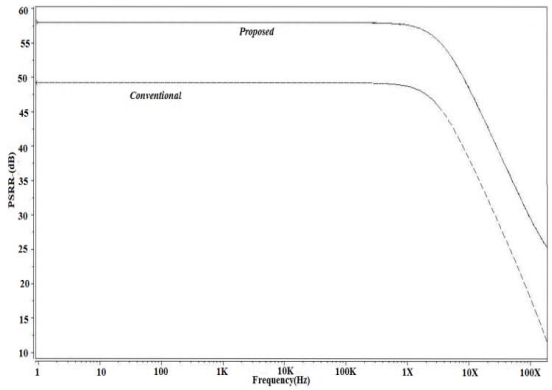
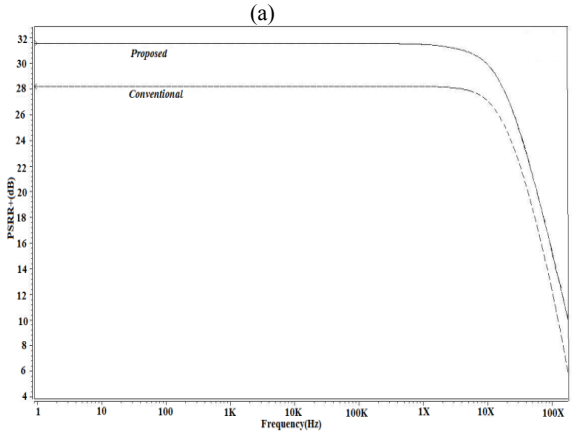


Figure 12: Gain frequency performances of the proposed and conventional differential amplifiers.



(a)



(b)

Figure 13: PSRR frequency performance of the proposed and conventional differential amplifiers a) PSRR- b) PSRR+.

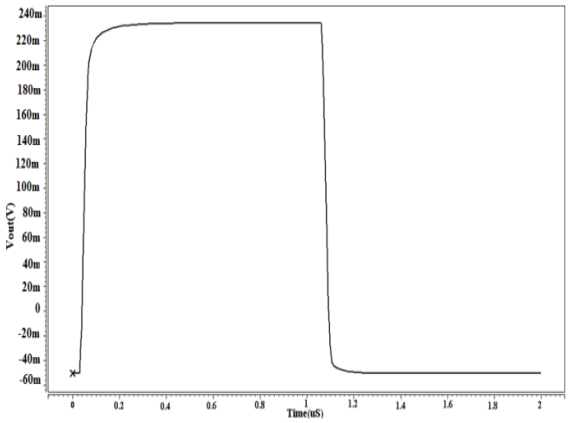
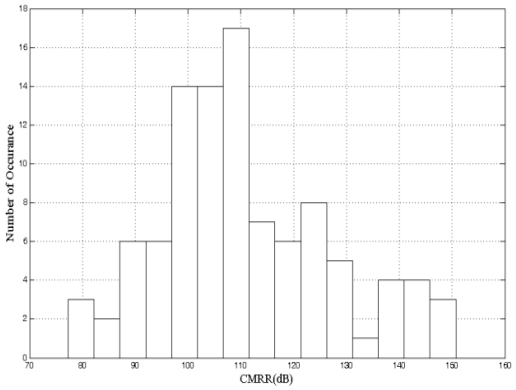
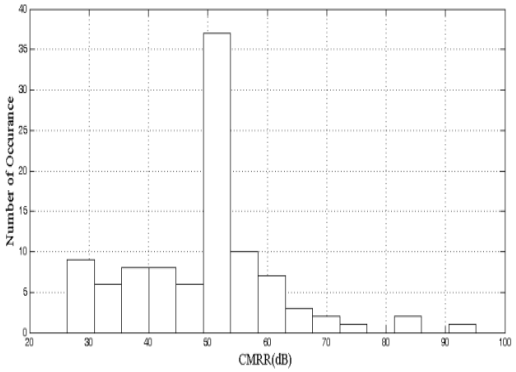


Figure 14: Transient response of the proposed differential amplifier.



(a)



(b)

Figure 15: Statistical distribution of CMRR in presence of Mismatches in (a) proposed d.a. (b) conventional d.a..

TABLE 5
COMPARISON OF CHARACTRISTICS OF THE PROPOSED AND CONVENTIONAL DIFFERENTIAL AMPLIFIERS.

Parameter	Proposed	Conventional
CMRR (dB)	150	55.6
Ad(Vo/Vd)(dB)	31.6	28.2
GBW(Mhz)	95.8	58.9
Phase Margin(º)	71	66
Power Supply(v)	±0.55	±0.55
PSRR+/-(dB)	31.6/58	28.2/49.2
Input referred noise(nV/√Hz) at 100KHz	100.64	173.57
PD(µW)	44.65	42.44

TABLE 6
COMPARISON BETWEEN PROPOSED D.A AND SOME OTHER ADVAANCED WORKS.

	[15]	[23]	[24]	This Work
Technology(µm)	0.5	0.5	0.5	0.18
Supply voltage(V)	±1.1	±1.5	1.9	±0.55
ICMR(V)	2	3	1.9	1.1
DC gain(dB)	63	89	44.7	31.6
CMRR(dB)	108	80	88	150
Power(µW)	410	510	62	44.6
Total capacitor used at the inputs (PF)	6	24	1.6	1.17
Configuration	Two stage	Two stage	Two stage	Single stage

4. CONCLUSION

With supply voltages becoming more limited, differential amplifiers input common mode range and common mode rejection ratio become extremely critical parameters. While MIFG and QFG transistors provide a very simple and accurate way to design low voltage and low power differential amplifiers, the resulted CMRR is relatively poor and gain bandwidth product is degraded. A novel low voltage low power rail to rail constant gm differential amplifier is introduced in this work. Its CMRR is improved over conventional one and some other reported works. Its gain bandwidth attenuation factor is reduced compared to that of the conventional d.a. and most other reported works. Moreover, the proposed d.a. has lower input referred noise compared to conventional one. Power efficient and compact structure of the proposed d.a. are other performance merits making it more suitable for low voltage low power designs. Power consumption is only 2.21µW larger than power consumption of conventional d.a. which along with other achievements makes the proposed d.a. an attractive alternative to conventional and other previously reported topologies. We have demonstrated by simulation a 94.4dB improvement in CMRR, 1.62 times improvement in gain bandwidth product, 1.72 time reduction of input referred noise and an improved power supply rejection ratio over that of the conventional differential amplifier.

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