

Amirkabir University of Technology (Tehran Polytechnic) Vol. 47, No. 2, Fall 2015, pp. 49- 60



Amirkabir International Journal of Science& Research (Electrical & Electronics Engineering) (AIJ-EEE)

The Impact of Superconducting Fault Current Limiter Locations on Voltage Sag in Power Distribution System

M. Ehsanipour¹, J.S. Moghani^{2*}, S.H. Hosseinian³ and M. Saberi⁴

1- MSc. Student, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

2- Associate Professor, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

3- Professor, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

4- MSc. Student, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

ABSTRACT

In this paper, the impacts of installing superconducting fault current limiter (SFCL) in radial and loop power distribution system are evaluated to improve voltage sag in both cases of with and without distributed generations (DG). Among various SFCLs, the hybrid type with a superconducting element in parallel with a current limiting reactor (CLR) is selected. This is more effective than resistor-type SFCLs because it reduces the burden on the superconducting element, ac losses and cost in distribution system. According to SFCLs impedance and their locations in power system, voltage sag will be improved by reducing the fault current. In this paper, SFCLs with various arrangement and CLR magnitudes are installed in distribution system and improving the voltage sags on different buses are examined according to fault position. Area of severity (AOS) method and expected annual sag frequency (ESF) are used to analyze the voltage sag. The results show that installing SFCL can improve the voltage sags as well as fault current reduction in radial and loop distribution systems.

KEYWORDS

Superconducting Fault Current Limiter (SFCL), Voltage Sag, Radial and Loop Distribution System, Distributed Generation.

Corresponding Author, Email: moghani@aut.ac.ir

1- INTRODUCTION

Over the past decades, different techniques using the characteristics of superconductors have been developed in many countries. In particular, superconducting fault current limiters (SFCL) have been developed as the most promising and suitable method for limiting the fault current in distribution systems. SFCL decreases the fault current and its adverse effects on power system and ultimately can reduce the capacity of circuit breakers. Moreover, SFCL can provide additional advantage as the improvement of voltage sags [1].

Power quality problems are becoming more and more important for electric utilities due to growing number of sensitive loads. Among these problems, voltage sag and momentary interruptions are serious problems that industrial and commercial customers face, and must be compensated [2]. It is shown that 80–90% of customer's displeasure is due to voltage sags that is mainly caused by short circuits in distribution system [3,4]. The sensitive loads can be protected from voltage sag by DVR and UPQC. However, these devices can only compensate the voltage sag of sensitive loads and they cannot affect the fault current. Therefore adding fault current limiters not only reduces the large fault current but also improves the reliability, stability, and the system power quality [5-7].

In [1] the effect of SFCL on voltage sag in a radial distribution system is presented by using the Information of Technology Industry Council (ITIC) curve. In [2] the various CLR magnitude in trigger-type SFCL on voltage sag in radial systems are presented. In [9] and [10] the improvement of superconducting fault current limiters on voltage sag is demonstrated. In [11] the effect of SFCL on voltage sag in loop distribution systems is presented. Nevertheless, the impact of SFCL on voltage sag frequency and reduction of fault current has not been investigated in recent research activities.

Voltage sag is evaluated by magnitude and duration. In general, SFCL can improve the magnitude of voltage sag, whereas it may worsen the duration of voltage sag because it reduces fault current and increases the delayed trip time of protective devices [12]. In addition, distribution system is being changed to the loop system in microgrids or smartgrids. Therefore, the impacts of SFCLs impedance and their position in radial and loop distribution systems and microgrids on voltage sags should be analyzed with various fault locations and in this paper has been covered mentioned lacks of studies.

The rest of this paper is followed as: In Section 2, we model a hybrid SFCL. In Section 3, the AOS and the annual expected sag frequency (ESF) (i.e. the expected number of voltage sags exceeds the voltage threshold) are

determined. In Section 4, FCRI (Fault Current Reduction Index) is introduced to evaluate the fault current reduction. In Section 5, ESF and FCRI are calculated using DPL. In Section 6, the impact of SFCLs arrangement on voltage sag and fault current reduction is evaluated in distribution system with and without DGs.

2- HYBRID SFCL

Several SFCL models have been developed. In this paper, the hybrid SFCL based on studies for hybrid SFCL being applied to Korean distribution systems is used [13-15]. In hybrid SFCL the size of superconducting material is reduced, therefore recovery time of superconducting element will be small and it can provide the reclosing operation of the power system without adverse effects. In addition, it economically would be appropriate. In hybrid SFCL, HTS element is used only to identify fault current and commutate the fault current into the driving coil and a resistor type or reactor type CLR is used for reducing fault current.

As can be seen in Fig. 1, the hybrid SFCL consists of a HTS element, driving coil, fast switch and a current limiting reactor (CLR). The paths for flowing fault current are shown in Fig. 1 and is illustrated performance of SFCL [16, 17].

Path 1: In normal state, flowing current through HTS is less than its critical current and its resistance is zero.

Path 2: When a short circuit occurs and the HTS current is higher than HTS critical current, the HTS is quenched and the HTS resistance increases in the quenching state based on (1). Then, currents of over 90% of the total current detour through the driving coil.

Path 3: When the current flows through the driving coil it will trigger contact-1 and contact-2. However, contact-1 is mechanically opened, but it is still electrically closed due to arcing.

Path 4: Contact-1 becomes electrically open, when the electric arc on the contact is removed and the fault current flows through the CLR to be limited [18, 19].

$$R_{SFCL}(t) = \begin{cases} 0, & (t_0 > t) \\ R_m \left[1 - exp\left(-\frac{t - t_0}{T_{SC}} \right) \right]^{0.5}, & (t_0 \le t \le t_1) \\ a_1(t - t_1) + b_1, & (t_1 \le t \le t_2) \\ a_2(t - t_2) + b_2, & (t_2 \le t) \end{cases}$$
(1)

In (1), R_m , T_{SC} , t_0 , t_1 and t_2 represent the maximum resistance of HTS in quenching time, HTS time constant, quench-starting time, first recovery starting-time and second recovery starting-time, respectively. The used SFCL parameters are shown in Table 1.



Fig. 1. Current flow paths of the hybrid SFCL at normal and fault conditions.

TABLE 1

Parameter	Value	Unit
Nominal voltage	25	kV
Nominal current	300	Arms
Critical current (I _{critical})	450	Arms
HTS recovery time	50>	ms
R _m	0.6	Ω
T _{SC}	0.01	S
a_1, a_2	-80, -160	1/s
b ₂	0.3	Ω

as follows:

HYBRID SFCL PARAMETERS

Based on results in [1,11], resistive type SFCL has better performance on improvement of voltage sag. Therefore, in this paper the hybrid SFCL with resistive CLR is used to improve voltage sag.

3- AOS AND ESF CALCULATION

The occurrence of a fault in the power system may cause voltage sag which affects the performance of sensitive loads. The AOS is defined as the region of the power system where the occurrence of faults will simultaneously lead to voltage sags at different sensitive load points. In general the ESF is calculated by multiplying bus fault rate and line fault rate in number of buses and the total length of lines in areas of vulnerability. Because three phase fault is the most severe

$$F(SL)_{BF} = \sum_{B \in ABSL} BFR_{3PH} + \sum_{L \in ALSL} l_L \times LFR_{3PH}$$
⁽²⁾

fault and has maximum fault current in the power system,

in this paper three-phase fault is studied. The ESF for the

severity level (SL) for the three-phase fault is calculated

TABLE 2	
SYSTEM 3Ph FAULT RATE FOR BUSES ANI) LINES

Bus fault rate, event/year	Line fault rate, event/100 km/year
0.004	0.168

TABLE 3

PARAMETERS OF THE DISTRIBUTION SYSTEM MODEL

Transformer	Voltage	Ca	pacity
TR1	120-25 kV	20 MVA	
TR2	575 V-25 kV	10	MVA
TR3, TR4	230 V-25 kV	2 MVA	
DG1 (wind)	575 V	6 MW	
DG2, DG3 (PV)	230V	1 MW	
load	P (MW)	Q (MVAR)	
L1	2.0	0.6	
L2, L3	1.5	0.3	
L4, L5	1.0	0.2	
Distribution lines	R0, R1 (Ω/km)	L0, L1 (H/km)	C0, C1 (F/km)
DL1, DL2, DL3, DL4, DL 5	0.1153, 0.413	1.05e-3, 3.32e-3	11.33e-9, 5.01e-9



Fig. 2. Distribution system model.

where B is the system bus, L the system line, I_L the length of line L inside the AOS_{SL}, ABSL and ALSL are the set of all buses and all lines inside the AOS_{SL}, BFR_{3Ph} and LFR_{3Ph} are the bus and the line fault rate for three phase fault. The 3Ph bus fault rate and line fault rate are listed in Table 2 [18]. We used uniform distribution of faults along the line and to achieve accurate results, 3Ph fault is applied at each 1% of the line length. Then, critical line length and the area of vulnerability for each bus in system are determined by considering severity level for each bus and finally ESF is calculated. In this paper, the area of vulnerability is considered for voltage threshold 0.7 p.u.

4- FAULT CURRENT REDUCTION INDEX (FCRI)

The fault current reduction index is defined as jth protective device fault current deviation in a power system with and without SFCL. The FCRI related to the



Fig. 3. (a) B-1 voltage waveform, (b) DL_1 line current waveform, when fault occurs in the middle of the line DL_1 with and without SFCL.

reduction in average fault current due to the installation of SFCL can be expressed as follows:

$$FCRI = \sum_{j=1}^{N_D} \omega_j \left(I_j^{WithoutSFCL} - I_j^{WithSFCL} \right)$$
(3)

where N_D is the total number of protective devices, $I_j^{WithoutSFCL}$ and $I_j^{WithSFCL}$ are fault current flowing through jth protective device with and without SFCL, respectively. The \mathcal{O}_j is weighting factor for jth device among the total number of devices N_D , which is calculated by the devices costs [20].

5- CASE STUDY

Fig. 2 represents the distribution system model with three DGs and four SFCL arrangements. Table 3 shows the parameters data of Fig. 2.

The voltage sag generally is caused by faults in the power system. When a fault occurs in the power system, consumers in each bus will experience different voltage magnitude due to various factors, such as line impedance, fault location, fault type and so on.

In order to investigate the impact of different SFCL arrangements and impedance on voltage sag and reduction in fault current, various SFCL arrangements are proposed in the distribution system in Fig. 2 (The numbers in the rectangles represent the SFCL installation arrangement). The voltage sag and fault current reduction have been investigated in the system with and without DGs. As depicted in Fig. 2, four arrangements for installing SFCLs are considered in this system. To assess the impact of SFCL impedance on voltage sag and fault current reduction, the CLR resistance is varied from 1 Ω to 4 Ω in different conditions and then ESF and FCRI are calculated.

Fig. 3 shows the voltage waveform for phase A for B-1 bus and fault current flowing through the DL_1 line when fault occurs in the middle of the line DL_1, without SFCL and with SFCL in first arrangement and the CLR resistance of 4Ω , when both CB_LOOP1 and CB_LOOP2 are open. In this case, the voltage magnitude is improved from 30.93% to 73.43% during fault and the impact of SFCL on improving voltage sag magnitude for bus B-1 is well defined.

When a temporary fault occurs in power system, the reclosers will operate, momentary interruption will occur, and all busses experience voltage sag. However, if a permanent fault occurs, the reclosing operations will be failed and circuit breakers should separate the faulted line from power system. This paper only examines the impact of faults on voltage sag magnitude.

For performance of system as loop distribution system, two CB_LOOP1 and CB_LOOP2 circuit breakers are considered. Therefore, four different modes are considered to evaluate the performance of system for analyzing voltage sag. In first mode both CBs are open, in second mode, CB1 is close and CB2 is open, in third mode, CB1 is open and CB2 is close and finally, in fourth mode, both CBs are closed.

6- ESF AND FCRI CALCULATION USING DPL

Calculating critical distance and vulnerability area in power system is difficult and is not applicable to a variety of systems. Therefore, a method should be used to determine the vulnerability area for different systems.

In this paper, the DPL (DIgSILENT Programming Language) is used in order to simplify the simulation and calculation process. DPL is an object-oriented programming language that can access any element as an object. Therefore, by using this feature, all elements in system (including transmission lines, generators, etc.), load flow and short circuit calculation can be defined as an object in the DPL environment and it can be used in power quality and reliability studies. In addition, DPL is able to analyze any structure of power system from simple network to radial and loop distribution system and in each voltage level of distribution, subtransmission and transmission systems.

The voltage sag generally happens from fault. Short circuit could be occur anywhere in the power system and voltage sag will continue until the protective devices clear the fault. Thus, the analytical tool we need to apply short circuit in any location in power system and it would be achieved by means of DPL programming language.

To determine the area of vulnerability for each bus, short circuit event should apply in all lines and buses in the system. The steps of program in DPL are depicted in flowchart in Fig. 4.

According to this flowchart, firstly all lines on the system are defined as a variable set (a set of objects) and the bus voltage at which the sensitive load connected (VPCC) is defined as an object variable. Then, the short circuit is applied in each percent of lines and on buses and in each step, the PCC voltage is measured and SFCLs current should be measured and compared with critical current (I_{crit}) to determine their resistance. Then when short circuit occurs at the parts of system where the PCC voltage gets less than the critical voltage (here 0.7 p.u) is selected to determine the area of vulnerability. In the final step, where all lines were evaluated, critical distance (exposure length) is determined for all buses in the system.

To calculate FCRI it is necessary to measure the fault current through protective devices in any fault event. As the same way DPL is used to obtain FCRI, in each fault event, the current through the protective devices is measured before and after installing SFCLs and FCRI is calculated.



Fig.4. Flowchart for calculating ESF and FCRI in DPL.

(a)			ESF		
Arrangement	NO SFCL	1 Ω	2 Ω	3 Ω	4 Ω
1	1.116	1.101	1.070	0.991	0.663
2	1.116	1.101	1.070	0.991	0.663
3	1.116	1.079	1.069	0.991	0.831
4	1.116	1.101	1.070	0.991	0.663

TABLE 4SUM OF ESF FOR ALL BUSES, a) WITHOUT DGS, b) WITH DGS.

(b) ESF Arrangement NO SFCL 1Ω 2Ω 3Ω 400.957 0.915 0.752 0.663 0.662 1 0.957 2 0.915 0.752 0.663 0.662 3 0.957 0.921 0.886 0.831 0.828 4 0.957 0.925 0.760 0.663 0.662

TABLE 5

FCRI VALUES, a) WITHOUT DGS, b) WITH DGS.

(a)	FCRI			
Arrangement	1 Ω	2 Ω	3 Ω	4 Ω
1	1.183	2.817	4.590	6.325
2	1.183	2.817	4.590	6.325
3	1.017	2.407	3.873	5.251
4	1.183	2.817	4.590	6.325

(b)	FCRI			
Arrangement	1 Ω	2 Ω	3 Ω	4 Ω
1	2.962	6.828	10.608	14.094
2	2.962	6.828	10.608	14.094
3	2.543	5.838	8.969	11.652
4	3.133	7.034	10.489	13.401

In Tables 4 and 5, the sum of ESF for all buses and FCRI are shown for all SFCL arrangements, and in case with and without DGs and for CB1 and CB2 modes.

It should be noted that all SFCL in four above arrangements, in every fault event do not quench and limit fault current because in every event current through it does not exceed HTS critical current. For example, when a fault occurs in middle of DL-3 and CB1 and CB2 are open, the fault current flowing through DL-1 in series with SFCL, is less than HTS critical current, thus its resistance still remains zero and has no impact on improving voltage sag and fault current reduction.

7- BEST ARRANGEMENT SELECTION

In section 5, the results of various SFCL arrangements and their impacts on voltage sag for all buses and fault current reduction were investigated. According to the Tables 4 and 5 it is noted that all SFCL arrangements have positive impact on improvement of voltage sag and fault current reduction. In addition, it is clear that increasing CLR resistance has better impact on ESF and FCRI.

However, it is useful to know that which arrangement is suitable regarding the modes of CBs and the operation of distribution system in all structures. This distribution system can operate in four different structures according to modes of CBs: both of CBs are open, case1, CB1 is close and CB2 is open, case2, CB1 is open and CB2 is close, case3, and both of them are close, case4. The percentage of operation time of system in each case are considered as 40% in case1, 25% in case2, 10% in case3 and 25% in case4. Finally, the best arrangement can be chosen by using improvement factor of ESF (*ESF*_{*IF*}) and improvement factor of FCRI (*FCRI*_{*IF*}) which are introduced in (4) and (5).

$$ESF_{IF} = \frac{\sum_{i=1}^{4} k_i ESF_{min}}{\sum_{i=1}^{4} k_i ESF_0}$$
(4)

where i is four modes of CBs operation and k_i is system operation time in mode i. ESF_{min} is the best (minimum) value of ESF with considering CLR resistance in each arrangement and ESF_0 is ESF value when SFCL is not installed in this distribution system.

$$FCRI_{IF} = \sum_{i=1}^{4} k_i FCRI_{max}$$
(5)

where $FCRI_{max}$ is the best (maximum) value of FCRI with considering CLR resistance in each arrangement.

 ESF_{IF} and $FCRI_{IF}$ values for each arrangement, with and without DGs are shown in Table 6 and 7. In order to examine the impact of SFCL installation on voltage sag, the ESF_{IF} is expressed as percentage. For example, if SFCLs install in second arrangement and with CLR resistance of 4 Ω , the number of annual voltage sag will be reduced by 22.33%. Therefore, decreasing the ESF_{IF} means more reduction in number of annual voltage sags in power system after installing SFCL. As well as increasing $FCRI_{IF}$, means better performance of SFCLs to reduce fault current flowing through protective devices in power system.

TABLE 6

${\it ESF}_{\it IF}\,$ VALUES IN CASE WITH AND WITHOUT DGS.

ESF _{IF} (%)	Without DGs	With DGs
Arrangement 1	20.96	16.55
Arrangement 2	22.33	25.23
Arrangement 3	13.97	10.41
Arrangement 4	20.96	15.07

TABLE 7

$FCRI_{IF}$ values in case with and without dgs.

FCRI _{IF} (%)	Without DGs	With DGs
Arrangement 1	3.616	8.098
Arrangement 2	3.957	12.179
Arrangement 3	4.153	7.061
Arrangement 4	3.616	7.281



Fig. 5. Exposure length for all buses without DGs. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.



Fig. 6. Exposure length for all buses with DGs. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4.

As seen in Table 6 and 7, second arrangement has better performance on voltage sag in both cases with and without DGs. In terms of improving fault current reduction index, second arrangement has better performance, too. It should be noted that the arrangement 1 includes two SFCLs and the arrangement 2 includes three SFCLs.

The critical distance or exposure length for all buses in system without SFCLs and with SFCLs in arrangement 2 and for all CBs modes, without DGs and with DGs are shown in Fig. 5 and Fig. 6.

The Impact of Superconducting Fault Current Limiter Locations on Voltage Sag in Power Distribution System

As seen in Fig. 6, installing DGs can improve voltage sag by reducing exposure length and ESF, however in this case fault current will be increased. Using SFCL could reduce fault current and solve this problem. In addition, SFCL can reduce exposure length and ESF. It means if SFCLs are installed in appropriate positions it could improve voltage sag in power system in both cases of with and without DGs. However, according to results, installing SFCL in loop distribution system has lower impact on improving the voltage sag in comparison with radial distribution system.

Therefore, if the main criteria is improving the voltage sag and reducing fault current, the arrangement 2 will be the best choice. Although economically the arrangement 1 is suitable because there are two SFCLs in this arrangement.

8- CONCLUSION

In this paper, various arrangements for installing SFCLs in radial and loop distribution system are analyzed for improving voltage sag by using the ESF index and reducing the fault current flowing through protective devices, with and without DGs. First, hybrid SFCL and radial/loop distribution system are modeled. Next, all fault cases are simulated by using DPL and the area of vulnerability is obtained to evaluate the voltage sag.

The simulation results show that voltage sag can be improved according to SFCLs location in power system as well as fault current reduction in both cases of with and without DGs. By considering simulation results it is shown that the second and first arrangement have more impact on improvement of ESF and FCRI, respectively. However, economically first arrangement is better because it has fewer SFCL.

REFERENCES

- [1] J. F. Moon, S. H. Lim, J. C. Kim and S. Y. Yun "Assessment of the impact of SFCL on voltage sags in power distribution system", IEEETrans. Appl. Supercond., vol. 21, no. 3, pp.2161 -2164 2011
- [2] Bollen Math hj. Understanding power quality problems voltage sag and interruption. New York: IEEE Press; 2000.
- [3] Recommended practice for monitoring electric power quality. IEEE Std. 1159, IEEE; 1995.
- [4] Ward DJ. Power quality and the security of electricity supply. Proc IEEE 2001; 89(12):1830–6.

- [5] S.-Y. Kim and J.-O. Kim "Reliability evaluation of distribution network with DG considering the reliability of protective devices affected by SFCL", IEEE Trans. Appl. Supercond., vol. 21, no. 5, pp.3561-3569 2011.
- [6] G. Didier , J. Leveque and A. Rezzoug "A novel approach to determine the optimal location of SFCL in electric power grid to improve power system stability", IEEE Trans. Power Syst., vol. 28, no. 2, pp.978 -984 2013.
- [7] Tosato F, Quaia S. Reducing voltage sags through fault current limitation. IEEE Trans Power Deliv 2001; 16(1):12–17S.
- [8] Jin-Seok Kim, Sung-Hun Lim, Jae-Chul Kim, and Jong-Fil Moon " A Study on Bus Voltage Sag Considering the Impedance of SFCL and Fault Conditions in Power Distribution Systems", IEEE Trans. Appl. Supercond., vol. 23, no. 3, 2013.
- [9] J. C. Das, "Limitations of fault-current limiters for expansion of electrical distribution systems," IEEE Trans. Ind. Appl., vol. 33, no. 4, pp. 1073–1082, Jul./Aug. 1997.
- [10] F. Tosato and S. Quaia, "Reducing voltage sags through fault current limitation," IEEE Trans. Power Del., vol. 16, no. 1, pp. 12–17, Jan. 2001
- [11] J.-F. Moon and J.-S. Kim "Voltage sag analysis in loop power distribution system with SFCL", IEEE Trans. Appl. Supercond., vol. 23, no. 3, 2013
- [12] J.-S. Kim, S.-H. Lim, and J.-C. Kim, "Comparative analysis on current limiting characteristics of hybrid Superconducting Fault Current Limiters (SFCLs) with first half cycle limiting and non-limiting operations," J. Elect. Eng. Technol., vol. 7, no. 5, pp. 659–663, 2012.
- [13] G.-H. Lee, K.-B. Park, J. Sim, Y.-G. Kim, I.-S. Oh, O.-B. Hyun and B.-W. Lee "Hybrid superconducting fault current limiter of the first half cycle non-limiting type", IEEE Trans. Appl. Superconduct., vol. 19, no. 3, pp.1888 -1891 2009.
- [14] O. B. Hyun, K. B. Park, J. Sim, H. R. Kim, S. W. Yim, and I. S. Oh, "Introduction of a hybrid SFCL in KEPCO grid and local points at issue," IEEE Trans. Appl. Supercond., vol. 19, no. 3, pp. 1946– 1949, Jun. 2009.
- [15] I. K. You, S. H. Lim, and J. C. Kim, "Operational characteristics of hybrid SFCL with first half cycle non-limiting operation considering its design parameter," IEEE Trans. Appl. Supercond., vol. 21, no. 3, pp. 1271–1274, Jun. 2011.
- [16] Ebrahimpour. M, Vahidi. B. Hosseinian. S.H. "A Hybrid Superconducting Fault Current Controller for DG Networks and Microgrids," IEEE Trans. Appl. Supercond., vol. 23, no. 5, OCT, 2013.

- [17] S. Lee, J. Yoon and B. Lee "Analysis model development and specification proposal ofhybrid superconducting fault current limiter (SFCL)", Proc.22nd Int. Symp. Superconductivity (ISS 2009), Physica C: Superconductivity, vol. 470, pp.1615 -1620 2010.
- [18] C.-H. Park, J.-H. Hong, G. Jang. Assessment of system voltage sag performance based on the concept of area of severity. IET Generation. Transmission and Distribution. 2010, 4(6):683-693.
- [19] PARK C.H., JANG G. 'Stochastic estimation of voltage sags in a large meshed network', IEEE Trans. Power Deliv, 2007, 22, pp. 1655–1664.
- [20] Hashemi, Y., Valipour, K., 2014. FDM based multiobjective optimal sitting and design of TC-FLSFCL for study of distribution system reliability. Int.J.Electr. Power61, 463 473.
- [21] S. Kar and S. R. Samantaray, "Time-frequency transform-based differential scheme for micro-grid protection," IET Generation Transmiss. Distrib, vol. 8, no. 2, pp. 310–320, Feb. 2013.