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A Class E Power Amplifier with Low Voltage Stress

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ABSTRACT

A new output structure for class E power amplifier (PA) is proposed in this paper. A series LC resonator circuit, tuned near the second harmonic of the operating frequency is added to the output circuit. This resonator causes low impedance at the second harmonic. The output circuit is designed to shape the switch voltage of the class E amplifier and lower the voltage stress of the transistor. The maximum switch voltage of the conventional class E PA is 3.56Vdc. However, higher switch voltage of about $4.5V_{DC}$ may be occurred, by considering nonlinear drain-to-source capacitance in class E PA. The obtained peak switch voltage of the designed class E PA is approximately 75% of the conventional one with the same conditions, which shows a significant reduction in peak switch voltage. MOSFET parasitic nonlinear gate-to-drain and nonlinear drain-to-source capacitances of the MOSFET body junction diode also affect the switch voltage in class E PA, which are considered in this paper. The actual MOSFETs have these parasitic capacitances; therefore, it is necessary to consider these elements in the design procedure. Reduced switch voltage in class E PA relaxes the breakdown voltage constraints of the active device. In the switch voltage of the designed circuit, the zero voltage and zero derivative switching (ZVS and ZVDS) conditions are satisfied. Simulation of the presented circuit is performed using PSpice and LTspice softwares. For verification of the designed circuit, the presented PA is fabricated and measured.

KEYWORDS

Class E Power Amplifier, Low Voltage Stress, MOSFET Parasitic Capacitances, ZVS and ZVDS Conditions.

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1- INTRODUCTION

Power amplifiers are high power-consuming elements in any communication system, so efficiency is a very important factor in the design process [1-2]. High efficiency power amplifiers have become one of the most significant components in the modern communication [3-4]. Switching mode power amplifiers are very high-efficiency amplifiers among the different classes of operations. One of the most important switching mode power amplifiers is class E PA, which is being used in power electronics and radio-frequency applications [5-6]. The class E PA was introduced in 1975 [7], which becomes popular due to high conversion efficiency and good performance in high frequencies. ZVS and ZVDS conditions in class E PA guarantee the switching loss, low noise and high efficiency at high frequencies [8]. The efficiency of the class E PA can approach 100 percent theoretically, due to its shape of the switch voltage and current waveforms which has no overlap in the time domain. Maximum switch voltage in conventional class E power amplifier is $3.56V_{DC}$ [7]. Several parameters can change the voltage stress in class E PA, for instance, the nonlinearity of drain-to-source MOSFET capacitance can increase the maximum switch voltage to about $4.5V_{DC}$ [9-16]. Hence, adding linear shunt capacitance in parallel with the drain-to-source capacitance will lower the maximum switch voltage of the class E power amplifier [13]. However, this method cannot reduce the voltage stress lower than $3.56V_{DC}$. The duty ratio can also affect the maximum switch voltage of the amplifier [14-15]. Increasing the duty ratio can reduce the maximum switch voltage of the class E amplifier. The peak switch voltage also depends on the DC supply voltage and the MOSFET type [16].

In practice, high maximum switch voltage is a limitation for designing the class E power amplifier. The peak switch voltage cannot exceed a significant value because of breakdown drain-to-source voltage of the MOSFET, which limits the output power of the PA. Besides, the high peak switch voltage results in a lower power output capability, considering constant peak switch current.

According to the mentioned disadvantages of high peak switch voltage, several methods have been presented to decrease this value. Zener diodes [17] or transformer with diode [18] are used in class E PA to reduce the peak switch voltage; however, a loss is occurred in the Zener diode. Inverse class E [19-20] and the E/F [21-22] family amplifiers have been introduced which lower the pick switch voltage, compared with the conventional class E PA.

The structure of inverse class E amplifier is symmetrical with class E PA, which can achieve 100 percent drain efficiency with zero current switching (ZCS) and zero current derivative switching (ZCDS) conditions under 50% duty ratio [23-24]. The Inverse class E peak switch voltage is approximately 20% lower than that of class E amplifier, which is $2.86V_{DC}$.

The E/F family amplifiers use control harmonic elements with class E amplifier structure. These amplifiers have been presented with reduced switch voltage compared to the conventional class E. However, the class E/F efficiency is lower compared to the class E PA. The ZVS and ZVDS conditions can also be satisfied in these amplifiers [22].

Sub-nominal class E amplifier can operate with lower peak switch voltage [25-26]. The class E power amplifier, which satisfies only the ZVS condition, is called the class E at sub-nominal condition, while the nominal condition requires both the ZVS and ZVDS conditions [20]. A flat top switch voltage class E PA is presented in [27] with 19% reduction in the maximum switch voltage. A parallel resonator tuned at second harmonic is added in the output path, after the conventional series resonator. More output power capability is achieved in this research; however, the output voltage waveform is not pure sinusoidal waveform.

A push-pull structure for class E power amplifier with a pair of LC resonant networks is designed in [28] with reduced peak switch voltage. Likewise, current mode class D amplifier has been introduced [29-30] with a lower switch voltage; however, current mode class D only achieves ZVS condition.

Reduced switch voltage leads to the lower transistor peak voltage, compared with the conventional class E. Hence, according to the reduced stress, more output power can be achieved with the same amount of stress [27]. Lower peak switch voltage also decreases the risk of the device failure due to the transistor breakdown mechanism and therefore, relaxes the breakdown voltage constraints of the active device [19].

This paper presents a low voltage stress class E power amplifier using a series LC resonator circuit, tuned near the second harmonic of the operating frequency. The aim of the design is to reduce the switch voltage of the class E power amplifier, using the presented control harmonic structure. The nonlinear drain-to-source and gate-to-drain capacitances are considered in simulation of the designed amplifier.

2- CONVENTIONAL CLASS E POWER AMPLIFIER

The Structure of conventional class E power amplifier is shown in Fig. 1. As can be seen from the figure, conventional class E PA consists of DC supply voltage (V_{DC}), a power MOSFET as a switching device, series resonant circuit (L_0 - C_0), shifting inductor (L_s), shunt capacitance, DC-feed inductance (L_{RFC}) and the load resistance (R). The shunt capacitance includes MOSFET intrinsic nonlinear drain-to-source capacitance (C_{ds}) and an external linear shunt capacitance (C_{ex}). In this paper, both C_{ex} and C_{ds} are considered in class E PA. The inductance L_s shifts the phase of the output current, while the resonant inductor L_0 with resonant capacitance C_0 form an series LC circuit to resonant in the operating frequency [16].

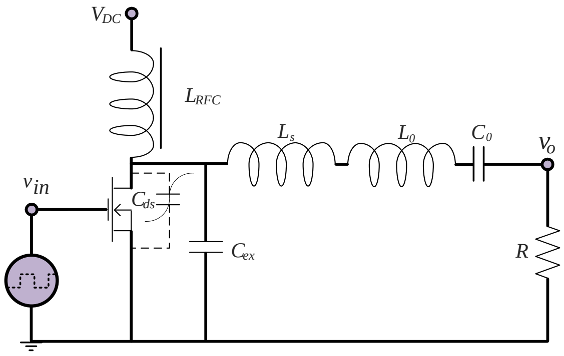

Fig. 1. Equivalent circuit of conventional class E power amplifier

Fig. 2 shows the simulated normalized switch voltage and output voltage waveforms of the conventional class E power amplifier circuit. As can be seen from Fig. 2, the peak switch voltage is $4V_{DC}$ in the simulated waveforms. This is because of the nonlinear drain-to-source capacitance which is in the MOSFET PSpice model. However, the external linear capacitance reduces the peak switch voltage. In other words, if the external capacitance is not considered in the circuit, the maximum switch voltage of the class E PA will be increased to about $4.5V_{DC}$.

3- STRUCTURE OF THE PRESENTED CLASS E AMPLIFIER

Fig. 3 shows the structure of the presented class E amplifier. In the presented structure, a series LC resonator circuit, tuned near the second harmonic of the operating frequency is added between the shifting inductance and series inductance. This series resonator makes a zero near the second harmonic of the operating frequency.

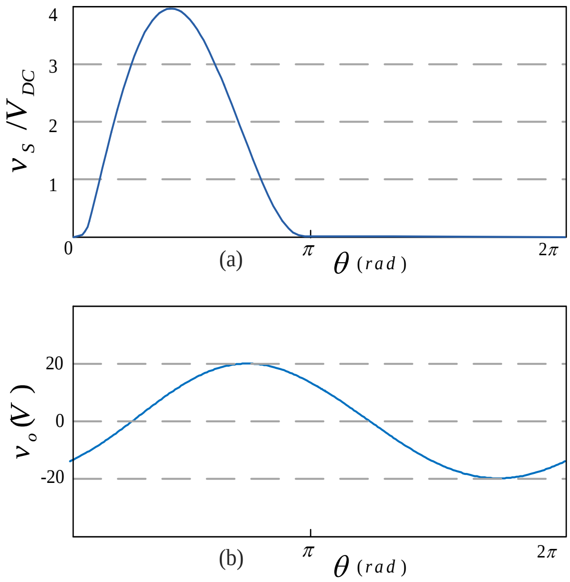

Fig. 2. Simulated waveforms of (a) normalized switch voltage and (b) output voltage for conventional class E power amplifier

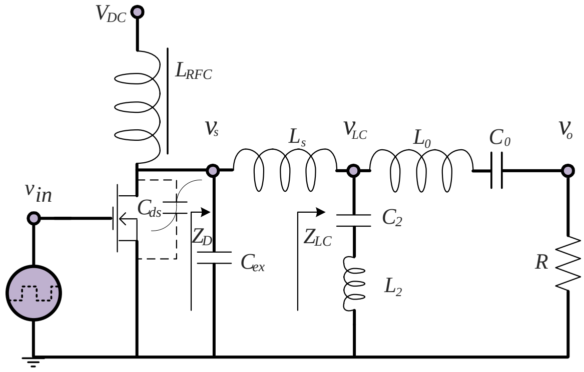

Fig. 3. Structure of the presented class E amplifier

The presented circuit is designed in such way that the impedance seen from drain will be low at first and second harmonics, while it will be large at the third harmonic. In other words, the load structure should make a pole at the third harmonic and two zeros at first and second harmonics. Therefore, the second harmonic is eliminated from the switch voltage and the third harmonic will be added to it. Consequently, the peak switch voltage will be reduced. The impedance of the output network, seen by the drain, when the switch is off, is shown in Fig. 4. However, the ZVS and ZVDS conditions can be satisfied, which result in high efficiency and zero switching loss at high frequencies in the designed class E PA.

The proposed structure shows different behaviour versus harmonics, compared with other switching amplifiers. A comparison between the presented structure and the other amplifiers versus harmonics is shown in Fig. 5. For the presented amplifier, at operating frequency the series L_0C_0 resonant circuit of the amplifier will be shorted and allows the fundamental component of the switch voltage to pass. The series L_2C_2 resonator will be shorted near the second harmonic, so the drain sees low impedance at this frequency. At the third harmonic, the drain sees the same lumped elements, but with different values, which cause high impedance. The series L_0C_0 resonant circuit is opened at second and third harmonics, so the resistant R will not seen by drain in these harmonics.

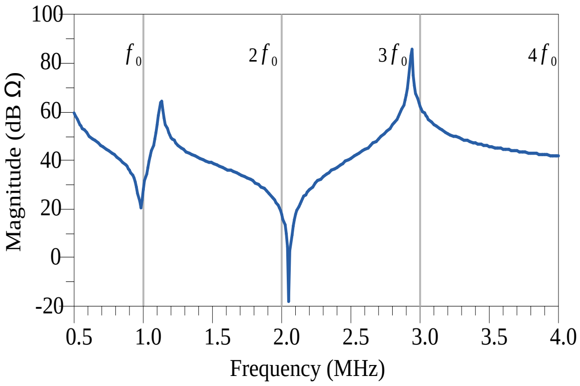

Fig. 4. Impedance of the output network seen by the drain, when the switch is off

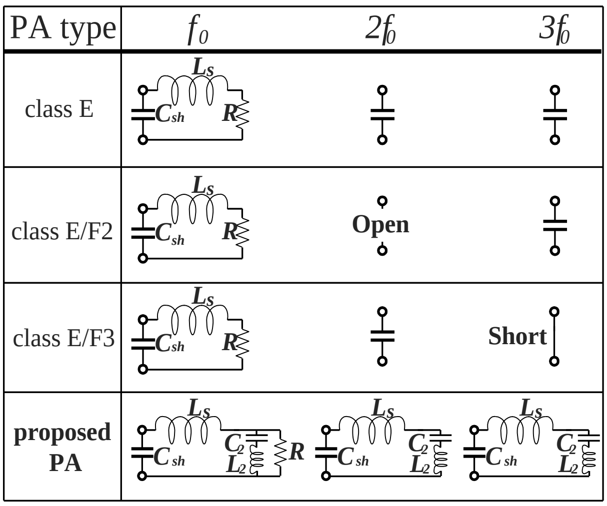

Fig. 5. Structures of different switching PAs versus harmonics

TABLE 1. PARAMETERS OF IRF530 AND IRFF510 MOSFETS

	C_{j0}	C_{gd}	C_{gs}	V_{bi}	V_{th}
IRF530	1151 pF	177.75 pF	596.15pF	0.8 V	3.2 V
IRF510	366.5pF	40.13pF	384.32pF	0.8 V	3.7 V

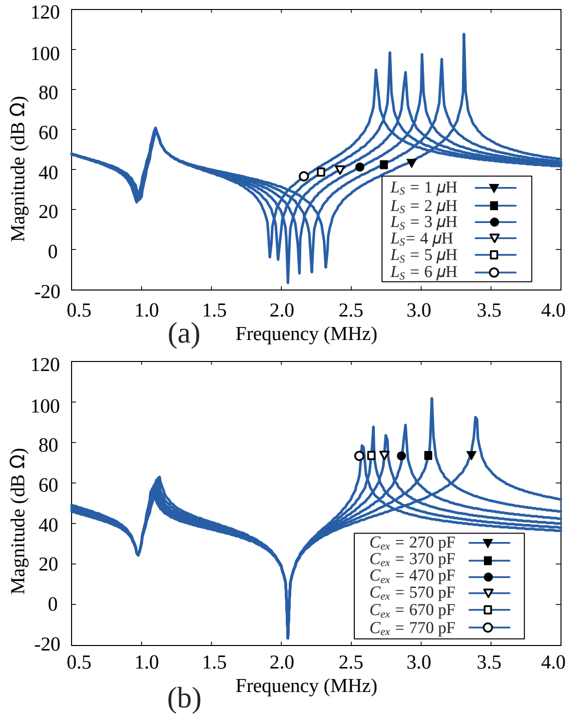

Fig. 6. The effects of (a) L_s and (b) C_{ex} on drain impedance

4- DESIGN PROCEDURE OF PRESENTED STRUCTURE

According to Fig. 3, the series resonant circuit, L_0C_0, should be shorted at the operating frequency, which is f_0=1 MHz. The value of L_0 can be obtained using the following equation: $L_0 = \frac{RQ}{\omega_0}$

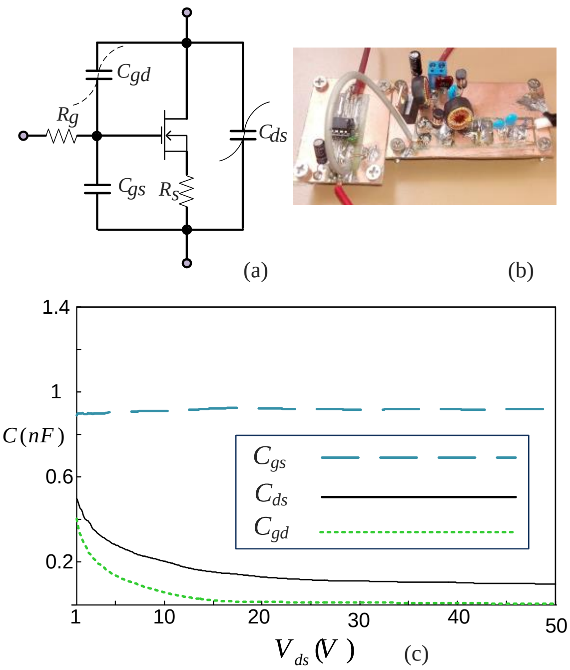

Fig. 7. (a) Simplified MOSFET model. (b) Fabricated circuit of the presented class E PA. (c) MOSFET parasitic gate-to-source, gate-to-drain and drain-to-source capacitances(1)

where Q is the loaded quality factor of the output resonant circuit. High value of Q is needed, due to the pure sinusoidal output waveform. The operating frequency can be written as

$$\omega_0 = \frac{1}{\sqrt{L_0 C_0}} \quad (2)$$

From (1) and (2), the value of C_0 can be achieved. The resonant circuit of L_2C_2 should make a zero at near the second harmonic, according to Fig. 4. Appropriate values of L_2 and C_2 are selected to provide low drain impedance near the second harmonic. The drain impedance can be written as:

$$Z_D = \frac{Z_{LC} + L_S S}{L_S C_{ex} S^2 + Z_{LC} C_{ex} S + 1}, \quad (3)$$

where Z_{LC} is the impedance of v_{LC} node, as shown in Fig. 3. Z_{LC} is defined as follows:

$$Z_{LC} = \frac{L_2 L_0 C_2 C_0 S^4 + R L_2 C_2 C_0 S^3 + (L_2 C_2 + L_0 C_0) S^2 + R C_0 S + 1}{(L_2 + L_0) C_2 C_0 S^3 + R C_2 C_0 S^2 + (C_2 + C_0) S} \quad (4)$$

Fig. 6 shows the drain impedance, which is obtained using (3) and (4). The effects of L_s and C_{ex} on drain impedance are also shown in Fig. 6. According to this figure, L_s changes the locations of zero and pole at second and third harmonics, respectively, while C_{ex} changes only the third harmonic pole location. Therefore, the values of L_s and C_{ex} should be selected according to the desired zero and pole locations, which are chosen 4 μH and 470 pF, respectively. The values of the obtained circuit elements are shown in Table 2.

5- SIMULATION AND EXPERIMENTAL RESULTS

MOSFET IRF530 is selected as a switching device in the designed amplifier. Parameters of IRF530 and IRF510 MOSFETs are extracted according to datasheet, which are given in Table 1. In fact, the actual MOSFETs have several parasitic components which should be considered in the design procedure. The simplified MOSFET model, which is used in this paper and the fabricated circuit of the presented class E PA, are shown in Figs. 7(a) and (b), respectively. The nonlinear drain-to-source capacitance is considered in PSpice MOSFET model, while the gate-to-source and gate-to-drain capacitance is considered to be linear. However, in LTspice MOSFET model, the drain-to-source and gate-to-drain capacitances are assumed nonlinear and the gate-to-source capacitance is considered linear. The calculated parasitic capacitances of MOSFET IRF530 are shown in Fig. 7(c), according to its datasheet information. As can be seen in this figure, the gate-to-source capacitance is approximately linear, while the drain-to-source and gate-to-drain capacitance are highly nonlinear, which affect the design specifications. The simulation results of switch voltage for designed amplifier, using PSpice and LTspice softwares are shown in Fig. 8. According to this figure, the maximum switch voltage of the designed amplifier is $3V_{DC}$ which is equal to 60 V. A significant reduction in switch voltage with the same output power has been achieved, compared with the conventional class E power amplifier peak switch voltage, which is shown in Fig. 2(a). The circuit is designed at the operating frequency f_0 = 1 MHz, duty cycle 0.5 and output power of 8.3 W. The values of the design specifications and obtained results for the proposed circuit are given in Table 2. The experimental and simulated waveforms of switch voltage (v_s) and output voltage (v_o) for the presented class E power amplifier are shown in Fig. 9. The simulation waveforms are obtained, using PSpice software. According to Fig. 9, the designed class E PA works in the nominal condition. The experimental and the simulated results are in good agreement.

6- CONCLUSION

A new structure for class E power amplifier was designed and fabricated. About 25% reduction of peak switch voltage was achieved, compared to the conventional class E power amplifier. The nominal operating conditions were achieved in the proposed structure, namely ZVS and ZVDS were satisfied. With the reduced peak switch voltage, higher output power can be achieved in class E power amplifier. The nonlinearity of drain-to-source and gate-to-drain MOSFET parasitic capacitances were considered in the design of presented amplifier. The simulations were performed using PSpice and LTspice softwares. A good agreement was observed between the experimental and the simulated results of the fabricated power amplifier

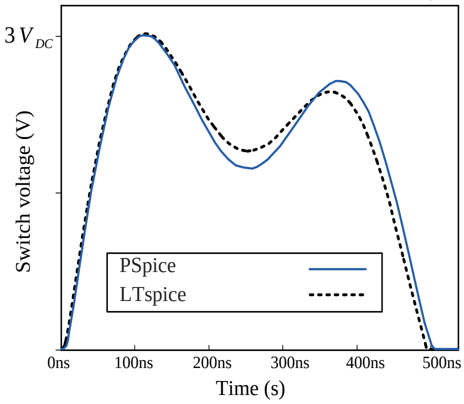

Fig. 8. Simulated switch voltage using PSpice (solid line) and LTspice (dashed line) softwares

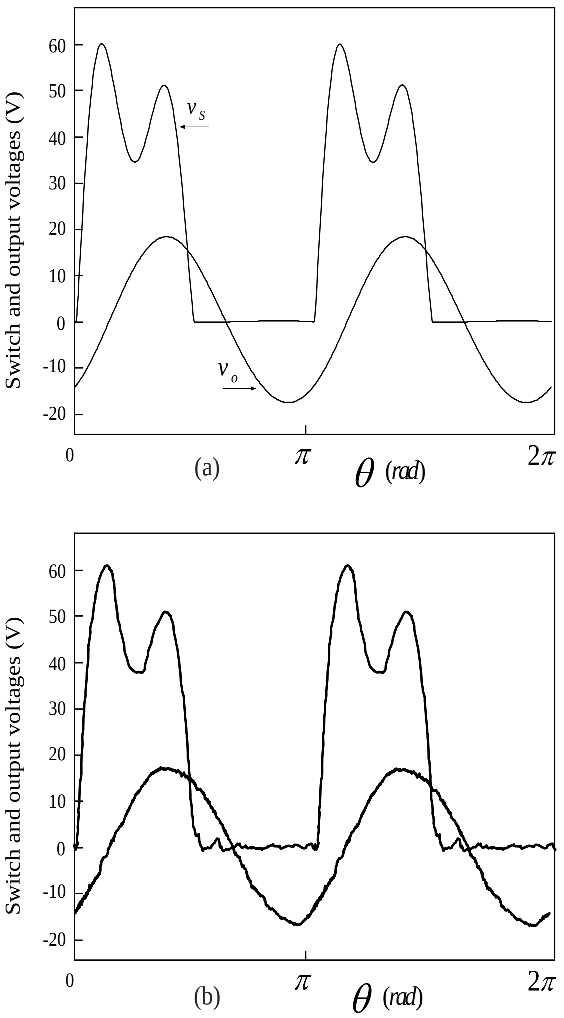

Fig. 9. (a) PSpice simulation and (b) experimental waveforms of the proposed class E power amplifier

TABLE 2. EXPERIMENTAL AND PSPICE SIMULATION RESULTS OF DESIGNED PA

	Simulation	Measured
V_{in}	10 V	10 V
V_{DC}	20 V	20 V
f_0	1 MHz	1 MHz
R	20 Ω	20 Ω
L_s	4 µH	4 µH
C_{ex}	470 pF	470 pF
L_0	107.8 µH	107.7 µH
C_0	235 pF	235 pF
L_2	9 µH	9.1 µH
C_2	470 pF	470 pF
L_{RFC}	100 µH	100 µH
$v_{s,max}$	60V	60.7 V
V_o	18.5 V	18.2 V
P_{out}	8.6 W	8.3 W

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