A Micropower Multi Decade Dynamic Range Current-Mode True RMS-to-DC Converter

Ebrahim Farshidi[i], Sayed Masoud Sayedi[ii]

ABSTRACT

A log-domain current-mode true RMS-to-DC converter based on a novel synthesis of a simplified current-mode low pass filter and a two-quadrant squarer/divider is presented. The circuit employs floating gate MOS (FG-MOS) transistors operating in weak inversion region. The converter features low power(<1.5uW), low supply voltage (0.9V), two quadrant input current, immunity from body effect, low circuit complexity, and very wide input dynamic range(0.7nA to 350nA). Simulation results by HSPICE show high performance of the circuit and confirm the validity of the proposed technique.

KEYWORDS

Current-mode, low-pass filter, floating gate MOS, RMS-to-DC converter.

1. INTRODUCTION

True RMS-to-DC converter as an electronic measuring circuit is used for estimation of the average energy content in an electronic signal. This converter is useful in biomedical ICs [1], instrumentation devices [2] and syllabic companding systems [3]. Recently, many integrated forms of this converter have been proposed. Some proposed design techniques are based on the bipolar dynamic translinear implementation [2], [4], [5]. However, in many situations, particularly in mixed A/D systems, it is desirable to implement the circuits in MOS technology. One technique is to employ sigma-delta converter [6], but the extra needed circuit leads to a large number of transistors and high power consumption. Up-down translinear loops and class-AB linear transconductors based on CMOS technology have been employed too [7], [8]. The main drawbacks of these proposed techniques are as follows: first, these circuits operate in only one quadrant input current, that means additional circuits for full-wave rectification is needed; secondly, the body effect of translinear MOSFETs in the squarer/divider block of these circuits decreases the accuracy[8]; thirdly, the low pass filter for time averaging operation requires construction of a complex circuit with many transistors; and finally, in these circuits employing low voltage restricts input dynamic range[4]-[9]. In this work, a new design to overcome the above problems is presented. A new synthesis with a squarer/divider circuit based on floating gate MOS transistors with two-quadrant input is implemented, so the full-wave rectifier is not required. Also, since the sources of the FG-MOSs are connected to the substrate, the proposed squarer/divider is immune to the body effect. Applying a novel synthesis, the time average operation is performed by a simplified current-mode low pass filter that is constructed by one capacitor and one MOS transistor. The complexity of this filter is much less than those proposed before [6]-[12]. Also, the proposed converter requires very low voltage with minimum of one V_{gs} plus one V_{ds}. Extra current and voltage biasing are not needed and the input dynamic range of the circuit is much wider than those proposed before [6]-[8].

The paper organized as follows. In section 2, the basic principle of operation of current-mode true RMS-to-DC converter and in section 3 the FG-MOS transistor as the basic element of the squarer/divider circuit are discussed. In section 4, analysis and synthesis of the proposed squarer/divider and low-pass filter as the basic building blocks of the converter are described. In section 5 a RMS-to-DC converter demonstrating the validity of the proposed method is presented. Simulation results and concluding remarks are presented in sections 6 and 7, respectively.

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2. BASIC PRINCIPLE OF RMS-TO-DC CONVERTER

The definition of the root mean square value of a signal with a period of T is given by:

$$I_{out}(t) = \sqrt{\frac{1}{T}\int_{t}^{t+T} I_{in}^{2}(t)dt} \quad (1)$$

in which $I_{in}(t)$ and $I_{out}(t)$ are the input and output currents of the RMS-to-DC converter, respectively. A mathematically equivalent expression, but more precise considering the offset of the system [4], is given by:

$$I_{out} = \left\langle \frac{I_{in}^{2}(t)}{I_{out}} \right\rangle \quad (2)$$

where $\langle ... \rangle$ represents the averaging operation.

Fig. 1 shows the block diagram of the current-mode true RMS-to-DC converter that consists of two separate functions: a squarer/divider and a first order low pass filter. The operation of the squaring/division can be done by using an electrically simulated translinear loop, with the help of floating gate MOSFET transistors, and the averaging operation can be done by using a first order current-mode low-pass filter (lossy integrator).

3. FLOATING GATE MOS TRANSISTOR

A floating gate MOS (FG-MOS) transistor with N input voltages $V_1, V_2, ..., V_N$ consists of a floating gate electrode extended over the channel and N input gates located over the floating gate. In other words, the FG-MOS transistor is a MOS transistor with an isolated gate that capacitively coupled to the inputs. Fig. 2 shows the symbol diagram and equivalent circuit of a p-type FG-MOS transistor with 3 input voltages.

Applying charge conservation law, the voltage at the floating gate is given by:

$$V_{FG} = \sum_{1}^{N} \frac{C_i}{C_t} V_i + \frac{C_{gd}}{C_t} V_{gd} + \frac{C_{gs}}{C_t} V_{gs} + \frac{C_{gb}}{C_t} V_{gb} + \frac{Q_{fg}}{C_t} \quad (3)$$

where C_i is the input capacitance between the floating gate and the i-th input, C_t is the total of these input capacitances, C_{gd}, C_{gs}, C_{gb} are the parasitic capacitors between the floating gate and the drain, source and bulk, respectively, and Q_{fg} is residual charge trapped at the floating gate during fabrication process. This latter charge can be made negligible by using the technique described in [13]. If the sum of input capacitances is much larger than parasitic capacitances, i.e.,

$$\sum_{1}^{N} C_i >> C_{gd}, C_{gs}, C_{gb} \quad (4)$$

then the voltage at floating gate can be approximated by:

$$V_{FG} \cong \sum_{1}^{N} \frac{C_i}{C_t} V_i \quad (5)$$

Thus, the drain current of a p-type FG-MOS transistor with N input gates, in weak inversion region is given by:

$$I_d = I_s \exp\left(\frac{1}{nU_T} \sum_{i=1}^{N} (V_{DD} - w_i V_i)\right) \quad (6)$$

where U_T is the thermal potential, I_s is a device dependent coefficient, n represents the subthreshold slope and w_i is input

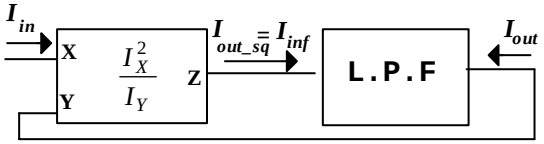


Figure 1: Block diagram of the RMS-to-DC converter.

capacitance ratio defined as:

$$w_i = \frac{C_i}{C_t} \quad (7)$$

4. SQUARER/DIVIDER AND LOW PASS FILTER CIRCUITS: ANALYSIS AND SYNTHESIS

A. Squarer/Divider Circuit

The squarer/divider can be implemented by using of sigma-delta data converter [3], MOS translinear [8], [12], [14] or class-AB tranconductance [7] circuits. Employing sigma-delta converter needs a large number of transistors, switches, and capacitors that leads to a high circuit complexity, chip area and power consumption [6]. MOS translinear circuits can be categorized as follows: stacked loop, up-down loop and electronically simulated loop [15]. The stacked loop [14] similar to class-AB tranconductance suffers from body effect. Influence of the body effect in up-down loop [8] is smaller than in stacked loop but more circuits for current injection in transistors are required. In the electronically simulated loop, the body effect is completely eliminated but a lot of additional circuitry is needed to force the two averages of the gate-source voltages of the loop be equal [12]. In addition, all these proposed squarer/divider circuits operate in only one quadrant input current. To make the input current of the squarer/divider operate in two-quadrant with positive and negative currents, a new synthesis by employing of FG-MOS transistors is presented. This will cause the squarer/divider to act as a full wave rectifier with large dynamic range and lower static power consumption. To this end, the input current I_{in} is split into its differential representation (I_{inp} , I_{inn}) which

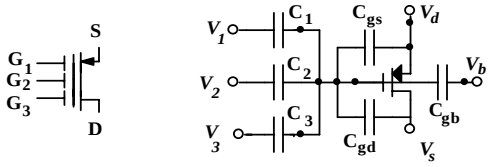
are both strictly positive and are related to I_{in} by:

$$I_{in} = I_{inp} - I_{inn} \tag{8}$$

Also the input-output relation of the squarer/divider block in current-mode is given by:

$$I_{out\_sq} = I_{in}^2 / I_{rms} \tag{9}$$

where I_{out_sq} is the output of the block, I_{in} is the squared input of the block (which is also equal to the input of the converter as shown in Fig. 1) and $I_{rms} = I_{out}$ is the divisor input of the block (which is also equal to the output of the converter and the filter as shown in Fig. 1). Using (8) and (9), it is obtained that:



(a) (b)

Figure 2: a: Symbol diagram and b: Equivalent circuit of a p-type FG-MOS.

$$I_{out\_sq} = \frac{(I_{inp} - I_{inn})^2}{I_{rms}} \rightarrow \tag{10}$$

$$I_{out\_sq} = \frac{I_{inp}^2}{I_{rms}} + \frac{I_{inn}^2}{I_{rms}} - 2\frac{I_{inp} I_{inn}}{I_{rms}}$$

The right hand side (RHS) of (10) consists of three one-quadrant functions: two squarer/dividers and one multiplier. For implementation of these functions, the p-type FG-MOS transistors are employed. Fig. 3 shows the circuit of a one-quadrant squarer/divider consisting of three FG-MOSs, where it is assumed all transistors are operating in weak inversion region. The I-V relationships for transistors M1, M2 and M3 are given by:

$$I_1 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{11}V_1 + w_{12}V_1\right)\right)\right) \tag{11}$$

$$I_2 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{21}V_2 + w_{22}V_2\right)\right)\right) \tag{12}$$

$$I_3 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{31}V_1 + w_{32}V_2\right)\right)\right) \tag{13}$$

Assuming that $w_{11} = w_{12} = w_{21} = w_{22} = w_{31} = w_{32} = 1/2$, squaring both sides of (13) and then substituting (11) and (12) into it, the following expression will be obtained:

$$I_3^2 = I_1 I_2 \rightarrow \quad I_1 = \frac{I_3^2}{I_2} \tag{14}$$

Therefore, a one-quadrant squarer/divider circuit is obtained by taking a copy of I_1 as the output, while I_2 and I_3 are as the inputs.

Fig. 4 shows the circuit of a one-quadrant multiplier which consists of four FG-MOSs that operate in weak inversion**.** The I-V relationships for transistors M1, M2, M3 and M4 are given by:

$$I_1 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{11}V_3 + w_{12}V_4\right)\right)\right) \tag{15}$$

$$I_2 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{21}V_2 + w_{22}V_2\right)\right)\right) \tag{16}$$

$$I_3 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{31}V_2 + w_{32}V_3\right)\right)\right) \tag{17}$$

$$I_4 = I_s \, exp\left(\frac{1}{nU_T}\left(V_{DD} - \left(w_{41}V_2 + w_{42}V_4\right)\right)\right) \tag{18}$$

By assumption that $w_{11} = w_{12} = w_{21} = w_{22} = w_{31} = w_{32} = w_{41} = w_{42} = 1/2$, from (15), (16), (17) and (18) it results:

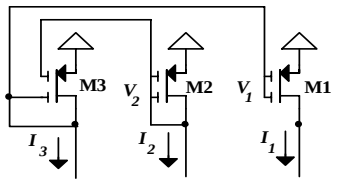


Figure 3: A FG-MOS based one-quadrant squarer/divider.

$$I_1 I_2 = I_3 I_4 \rightarrow \; I_1 = \frac{I_3 I_4}{I_2}. \tag{19}$$

Therefore, a one-quadrant multiplier circuit is obtained by taking a copy of I_1 as the output, and copies of I_2, I_3 and I_4 as the inputs.

The source and substrate of transistors of the two above mentioned circuits are connected to supply voltage so the effect of the body effect is completely eliminated. Also, the complexity of these two circuits is much lower than those of up-down and electronically simulated MOS translinear based circuits.

Fig. 5 shows the complete circuit of the proposed two-quadrant squarer/divider circuit which is implemented based on equations (8) and (10). Transistors M1, M4 and M5 and transistors M2, M4 and M6 of Fig. 5 form two one-quadrant squarer/dividers for implementation of the first and second terms of RHS of (10) according to Fig. 3. Transistors M3, M4, M5 and M6 form a one-quadrant multiplier. This multiplier and current mirror transistors (M9, M10) are employed for implementation of the third term of RHS of (10) according to Fig. 4. The common elements of these three circuits are merged. For implementation of (8)

transistors M5, M6, M7 and M8 are employed.

As Fig. 5 shows, the sources of FG-MOSs are connected to the substrate, so the body effect is completely eliminated. Also, the figure shows the minimum supply voltage of the circuit is one V_{gs} plus one V_{ds}, and since extra biasing current and voltage are not needed, the static power consumption is decreased. Since the FG-MOSs operate in weak inversion region, the power consumption is very low and dynamic range is large.

It should be pointed out that the RMS-DC converters that are based on the sigma-delta modulators [6] operate in voltage- mode. But for being used in the systems that work in

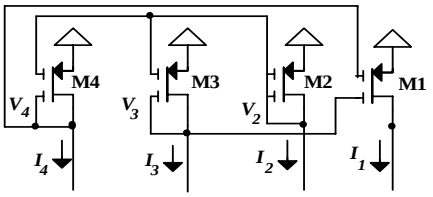


Figure 4: A FG-MOS based one-quadrant multiplier.

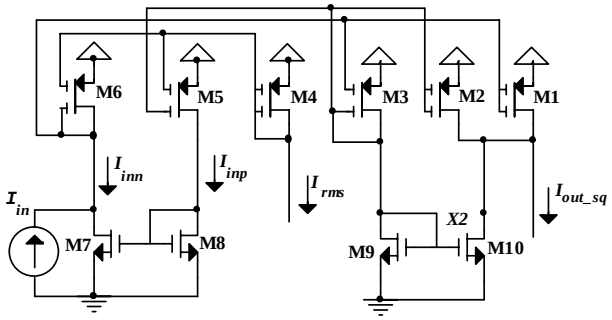


Figure 5: Circuit diagram of the two-quadrant squarer/divider.

the voltage-mode, the proposed converter and other existing current-mode RMS-DC converters [7], [8] need additional circuits for voltage-to-current converter at the input and current-to-voltage converter at the output. Also, the maximum operating frequency of the proposed converter with the MOS transistors that operate in the weak inversion is less than the frequency of the converters with MOS transistors that operate in the strong inversion [6], [7], [8].

B. Low Pass Filter Circuit

The current-mode filter of the RMS-to-DC converter can be implemented by using of switched capacitor [6], MOS translinear [8]-[12] or class-AB transconductance [7] circuits. In this paper, a simplified current-mode filter based on a novel synthesis is proposed. In Laplace domain the transfer function of the filter can be written as:

$$\frac{I_{outf}(s)}{I_{inf}(s)} = \frac{1}{1+\frac{s}{\omega_c}} \qquad (20)$$

in which ω_c is the cutoff frequency, $I_{outf}(s)$ is the output current and $I_{inf}(s)$ is the input current of the filter. Equation (20) in time domain can be written as:

$$\frac{dI_{outf}}{dt} = \omega_c\left(I_{inf} - I_{outf}\right) \qquad (21)$$

To implement the filter we use the circuit shown in Fig. 6 in which output current $I_{outf}(t)$ is nonlinearity related to a certain capacitor voltage $V_{cap}(t)$ by:

$$I_{outf} = I_S\, exp\left(\frac{V_{cap}}{nU_T}\right) \qquad (22)$$

Using equations (21) in (22) and also equation $I_{cap} = C\frac{dV_{cap}}{dt}$ result:

$$I_{cap} = \frac{nU_T C\omega_c}{I_{outf}}\left(I_{inf} - I_{outf}\right) \qquad . \qquad (23)$$

As shown before in Fig. 1, the output current of the filter I_{outf} is equal to the output current of the RMS-to-DC converter I_{out}, and the input current I_{inf} is equal to I_{in}^2 / I_{out}. Applying these two substitutions to (23) gives:

$$I_{cap} = \frac{nU_T C\omega_c}{I_{out}}\left(\frac{I_{in}^2}{I_{out}} - I_{out}\right) \qquad (24)$$

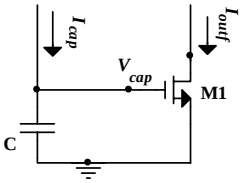


Figure 6: Current-mode SRD filter principle.

Considering the cutoff frequency of the filter as $\omega_c = I_{out} / nU_T C$, equation (24) can be rewritten as

$$I_{cap} = \left(\frac{I_{in}^2}{I_{out}} - I_{out}\right) \qquad (25)$$

Fig. 7 shows the proposed current-mode filter circuit based on equation (25), which consists of one capacitor and one transistor. It can be shown that the cutoff frequency of the filter is given by:

$$\omega_c = \frac{g_m}{C} \tag{26}$$

in which $g_m = \frac{\partial I_{out}}{\partial V_{gs,out}} = \frac{\langle I_{outf} \rangle}{nU_T}$ is the linear tranconductance of output transistor M1. Substituting g_m in (26) results:

$$\omega_c = \frac{\langle I_{outf} \rangle}{nU_T C} = \frac{\langle I_{out} \rangle}{nU_T C} \tag{27}$$

Eqn. (27) shows that the condition of ω_c considered on extraction of eqn. (25) is satisfied.

Comparing this filter with other proposed filters which are realized based on the switched capacitor technique [6] or is implemented by three translinear loops [8]-[12], or by two class-AB transconductors [7], shows that this analysis gives a much simpler circuit. To obtain this simple circuit, as equation $\omega_c = I_{out} / nU_T C$ indicates, the cutoff frequency of the filter is allowed to vary with output current. This dependency to I_{out}, and also the maximum acceptable output ripple determine the suitable values for capacitor C. This subject is discussed next.

The output current of the RMS-to-DC converter is a DC current $I_{true-RMS}$ with an ac ripple I_{ripple} on it. In order that converter gives a good performance the amplitude of this ripple should be small compared to $I_{true-RMS}$. This requires suitable values for the cutoff frequency of the filter.

As it is mentioned above, ω_c is proportional to the output current of the converter; however the value of the capacitor can be calculated in such a way that it eliminates the effect of this dependency and also achieves enough accuracy in the output of the converter. To this end, we first substitute $I_{in,f}$ and $I_{out,f}$ in (21) that results:

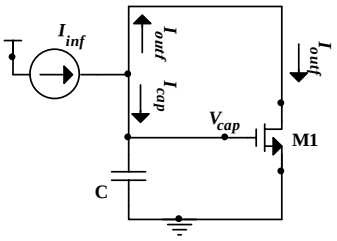


Figure 7: Circuit diagram of the proposed low pass filter.

$$\frac{dI_{out}}{dt} = \omega_c \left(\frac{I_{in}^2}{I_{out}} - I_{out} \right) \tag{28}$$

Multiplying both sides of eqn. (28) by I_{out} gives:

$$I_{out} \frac{dI_{out}}{dt} = \omega_c \left(I_{in}^2 - I_{out}^2 \right) \tag{29}$$

$$\rightarrow$$

$$\frac{d\left(I_{out}^2\right)}{dt} = 2\omega_c \left(I_{in}^2 - I_{out}^2 \right)$$

Eqn. (29) is time domain representation of a current-mode filter with input of I_{in}^2, output of I_{out}^2 and cutoff frequency of $2 \times \omega_c$. In Laplace domain, the equation can be rewritten as:

$$\frac{I_{out}^2(s)}{I_{in}^2(s)} = \frac{1}{1 + \frac{s}{2\omega_c}} \tag{30}$$

Assuming that the input current is a sinusoidal function we have:

$$I_{in} = \sqrt{2}\, I_{true-RMS} \cos(\omega t) \tag{31}$$

where ω is the frequency of the input current of the converter. Squaring both sides of eqn. (31) gives the input signal of (30) as follows:

$$I_{in}^2 = 2 I_{true-RMS}^2 \cos^2(\omega t) \rightarrow \tag{32}$$

$$I_{in}^2 = I_{true-RMS}^2 \left(1 + \cos(2\omega t)\right)$$

A low pass filtering method for solving I_{out} was presented in [16] and is adopted in our present analysis. Using input signal of eqn. (32) in low pass filter of eqn. (30) gives:

$$I_{out}^2 = I_{true-RMS}^2 \left(1 + B \cos(2\omega t + \phi)\right) \tag{33}$$

where

$$B = \frac{1}{\sqrt{1 + (2\omega / 2\omega_c)^2}} \quad \text{and} \quad \phi = -tg^{-1}\left(\frac{2\omega}{2\omega_c}\right). \tag{34}$$

Assuming that $\omega_c << \omega$ and using Taylor series expansion gives:

$$I_{out} = I_{true-RMS} \sqrt{\left(1 + B\cos(2\omega t + \phi)\right)}$$

$$\cong I_{true-RMS} \left(1 + \frac{B}{2}\cos(2\omega t + \phi) - \frac{B^2}{8}\cos^2(2\omega t + \phi) + \cdots \right)$$

$$\cong I_{true-RMS} \left(1 - \frac{B^2}{16} + \frac{B}{2}\cos(2\omega t + \phi) - \frac{B^2}{8}\cos(4\omega t + 2\phi) + \cdots \right). \tag{35}$$

From (35) RMS and peak-to-peak ripple values at the output current are expressed by:

$$I_{RMS,out} = \left(1 - \frac{B^2}{16}\right) I_{true-RMS} \quad \rightarrow \tag{36a}$$

$$I_{RMS\ ,out} = \left(1 - \frac{1/16}{1+\left(2\omega/2\omega_C\right)^2}\right) I_{true-RMS}$$

$$I_{ripple\ \ ,out} = \frac{B}{2} I_{true\ -RMS} \quad \rightarrow \quad (36b)$$

$$I_{ripple\ ,out} = \frac{1/2}{\sqrt{1+\left(2\omega/2\omega_C\right)^2}} I_{true-RMS}$$

From (36) it can be concluded that if the frequency of the input signal is at least five times bigger than the cutoff frequency of the filter $(\omega \geq 5\omega_c)$, then the accuracy of more than 1% can be obtained at the output.

Assuming ω_{min} as the lower end of the frequency range and $I_{true-RMS,max}$ as the higher end of the RMS of the input (output) current range, using (26), and considering condition $(\omega \geq 5\omega_c)$ results the values of the capacitor for achieving the accuracy of more than 1% as:

$$C \geq \frac{5I_{true-RMS,max}}{nU_T\omega_{min}} \quad (37)$$

More accuracy at the output of the converter can be achieved by decreasing the cutoff frequency of the filter by employing larger capacitances or reducing linear tranconductance according to equation (26).

5. Second-Order Effects

The expressions presented in the previous sections are valid by assumption that influences of the second-order effects that cause deviations from the ideal exponential-law behavior of MOS (or FG-MOS) transistors are negligible. The body effect is the change of the threshold voltage V_{th} caused by the source-to-substrate bias of MOS transistors. As it has already been mentioned, due to the fact that the source of all transistors in the electronically simulated translinear loop is connected to the substrate, the body effect is completely eliminated.

The channel-length modulation causes the drain current to be dependent on the drain voltage and its dependency is inversely proportional to the channel length L. Long channel transistors have been employed in our proposed circuit, to eliminate this effect. These large lengths also reduce the mobility degradation effects and conductance of transistors.

Contribution of parasitic capacitors C_{gd}, C_{gs} C_{gb} in FG-MOSs has minor effect on the operation of converter by choosing the input capacitances much larger than the parasitic capacitors [17].

Fabrication tolerance and process gradients lead to mismatch between transistor parameters. The mismatch between input capacitances of FG-MOS transistors is more important in squarer/divider block. The analytical effects of these mismatch is reported in [17] that demonstrates the increase of second and third harmonic distortion. If the converter uses a low-pass filter with cutoff frequency of much less than the input current frequency, the influence of mismatch is considerably reduced. This is shown in simulation results of mismatch effects in section 6.

6. Simulation Results

The complete circuit diagram of the proposed RMS-to-DC converter is depicted in Fig. 8. The circuit was designed by LEDIT and then post layout simulation using HSPICE with TSMC 0.35um CMOS process parameters, with $V_{th,n} \cong 0.54V$ and $V_{th,p} \cong -0.65$V. V_{dd} =0.9V and C=300nF were employed. The aspect ratio of the FG-MOS transistors (M1-M6) was chosen as 20um/10um and for the current-mirrors transistors (M7, M8, M9) and transistor (M10) the corresponding values were 10um/10um and 20um/10um respectively. For the output transistors (M11-M13) the aspect ratio was 60um/10um. Most SPICE simulators have convergence problems with floating nodes during the operating point calculations, so an N-input FG-MOS model presented in reference [18] is used for simulation. Fig. 9 shows the steady-state time response of the converter for a sinusoidal input current with 100nA peak-to-peak amplitude and 100 Hz frequency. Fig. 10 shows the output current relative error defined as:

Relative error=

$$\frac{I_{out}(theoretical) - I_{out}(simulated)}{I_{out}(theoritical)} * 100\% \quad (38)$$

for different amplitudes of the sinusoidal input current. The figure reveals that errors less than 3% can be found for input current amplitudes from 0.3nA to 350nA. This input range with low supply voltage is much wider than those reported before [6]-[8]. Fig. 11 shows the simulation result of relative error in output current affected by mismatching in the input capacitance ratio of individual transistors M3, M5 and M6 for a sinusoidal input current with 100nA peak-to-peak amplitude and 100 Hz frequency. As Fig. 11 shows, even by deviation of the ratios from -10% to +10% the relative error less than $\pm 1.5\%$ is resulted. It should be noted that deviation values of $\pm 10\%$ have been overestimated.

Simulation results showed the power consumption of 1.5uW for the maximum accepted input current (350nA).

To provide more insight into the technique proposed here, a comparison was made with formerly reported CMOS RMS-to-DC converters. Table 1 summarizes this comparison by showing some important parameters of the

converters.

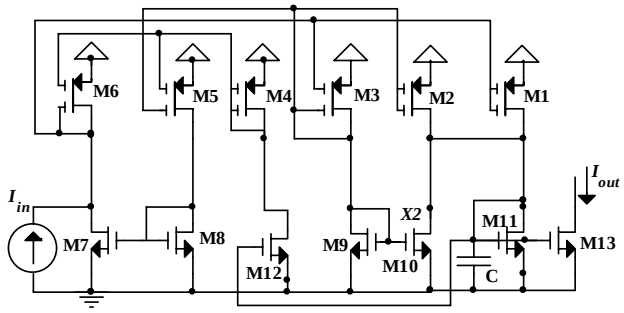


Figure 8: Complete circuit diagram of the RMS-to-DC converter

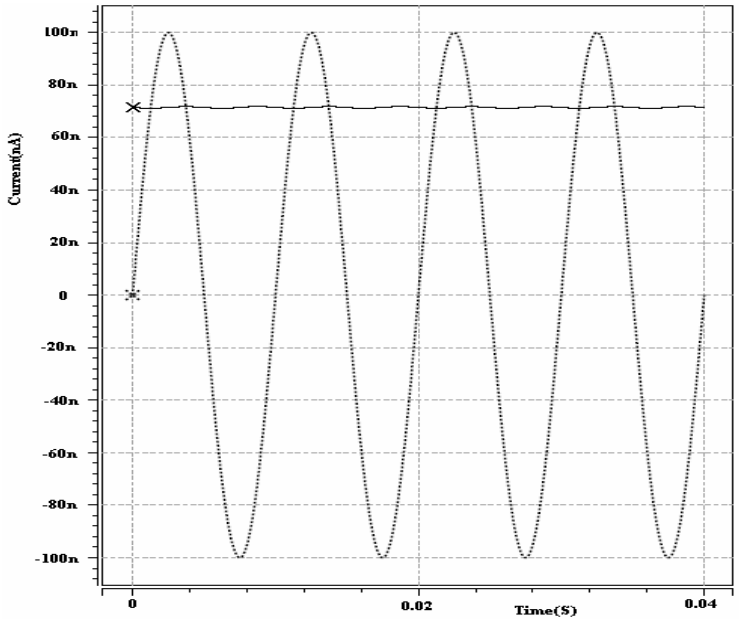


Figure 9: Time response of the input current (dotted) and output current (solid) of the RMS-to-DC converter.

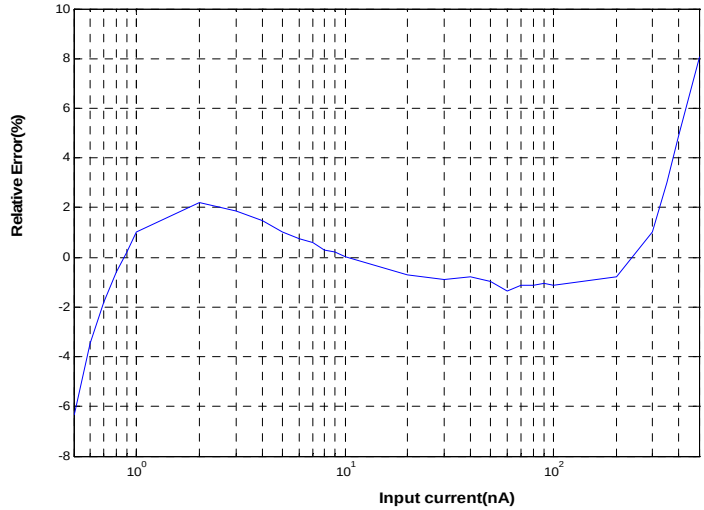


Figure 10: Relative error vs. input current amplitude of the RMS-to-DC converter.

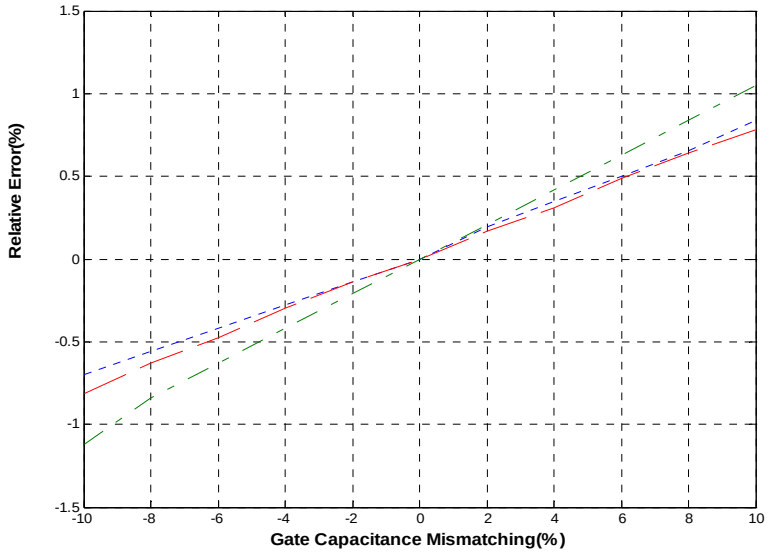


Figure 11: Relative error vs. mismatch input capacitances ratioof transistors M3 (dotted), M5 (dash-dot) and M6 (dashed).

TABLE 1
A COMPARISON BETWEEN RMS-TO-DC CONVERTERS.

	Converter[8]	Converter[7]	Converter[6]	This Work
Basic principle	MOS up-down translinear	Class-AB tranconductance	Sigma-Delta data converter	FG-MOS transistors
Technology	2.4u	0.5u	0.8u	0.35u
Minimum voltage	$V_{gs}+2V_{ds}$ (1.5V)	$V_{gs}+2V_{ds}$ (1.5V)	($\pm 3V$)	$V_{gs}+V_{ds}$ (0.9V)
Circuit complexity (Transistor number)	High (108 tr.)	Medium (40 tr.)	Very high (>>150)	Low (11)
Input current range	5uA-11uA @2%error	12uA-22uA @3%error	0.4V @2%error	0.7nA-350nA @3%error
Power consumption	Not reported but Expected >>100uW	> 200uW	40mW	< 2uW @400nA
Operation area of Input current	1 quadrant	1 quadrant	1 quadrant	2 quadrant
Influence of the Body Effect	Medium	High	Low	Zero
Operation mode	Current-mode	Current-mode	Voltage-mode	Current-mode

7. CONCLUSIONS

A two-quadrant squarer/divider circuit that employs FG-MOS transistors operating in weak inversion region is presented. The circuit that operates in two-quadrant input current is immune from body effect, works at low voltage and does not need to extra biasing to inject current into its transistors. Also, a new current-mode filter with low circuit complexity for time averaging is proposed. Simulation results of a RMS-to-DC converter, constructed based on the proposed squarer/divider and low-pass filter, show that the technique is promising and can be used in RMS measuring integrated circuits.

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